An Overview of the Performance Envelope of Digital Micromirror Device™ (DMD) Based Projection Display Systems

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Digital projection display systems based on the DMD utilize its silicon addressing circuitry and monolithic aluminum mirrors to achieve unique addressing modes, bit resolutions, pixel resolutions, aperture ratios, and color spaces in both three-chip and single chip configurations. This paper explores the range and implementation of each of these features.

Introduction

Recent advancers in DMD technology have been reported by several authors,[1-3] and this author reported the performance of a state-of-the-art front projection display system based on the DMD at the 1993 SID International Symposium[4]. That paper summarized in outline form the fabrication of the DMD and its mode of operation as a spatial light modulator (SLM) creating images using binary pulsewidth modulation of the "on" and "off" times of individual mirrors/pixels. Digital micromirror device development work at Texas Instruments in the intervening year has concentrated on characterizing and improving device resolution, reliability, manufacturability, and aperture ratio. The device has been further studied in projection display systems to better establish its color reproduction and contrast ratio capabilities.

This paper attempts to summarize some of the changes made in each of these areas between mid-1993 and mid-1994, and then predict what might be reasonable configurations and/or performance levels for DMDs in commercially viable display systems in the near term. Additionally, consideration is given to estimating what might represent ultimate performance limits for the device in its current implementation. The next sections of the paper discuss advances made in the fundamental mirror structure, developments in the silicon addressing circuitry that underlies the mirrors, and the fabrication of devices with pixel resolutions appropriate to high-resolution images.

Mirror Structure

The projector described in Reference 4 and shown at SID in 1993 used a 768 x 576 pixel DMD to show PAL or NTSC images with a contrast ratio of approximately 50:1 under optimum conditions. Obviously, in a front projection system, contrast ratio is limited by ambient illumination conditions, but it was believed that better ultimate contrast ratio performance was required in a commercially viable projection system. The DMD mirror structure in use in 1993 is shown in **Figure 1**. The structure is made entirely of aluminum and
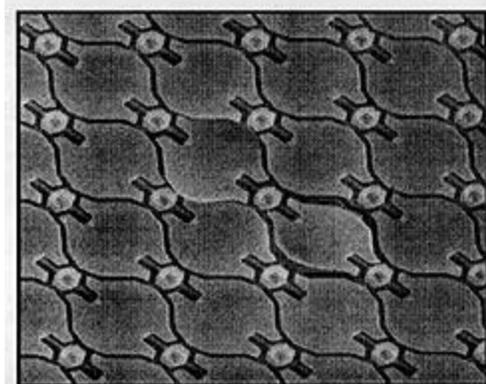

Fig. 1. A photomicrograph of a portion of a DMD mirror array fabricated through the use of a single sacrificial layer

formed using standard semiconductor deposition and etch techniques. Each mirror in the

x-y array of mirrors was suspended above an individual SRAM cell in an x-y array of memory cells by two thin metal torsion hinges attached to posts that are formed when the aluminum is sputtered onto a sacrificial polymer layer pierced by plasma etched vias. Electrostatic forces are created between the mirrors and address electrodes connected to the SRAM nodes at which the "1" or "0" voltages appear. These forces twist the mirrors one way or the other about an axis through the torsion hinges until the rotation is stopped at a precise angle determined by one mirror edge or the other touching the underlying substrate. Light modulation is achieved in a dark field projection system that discriminates between light reflected from mirrors tipped in one direction and those tipped in the other.

Typical mirror tilt is +/-10 degrees from a plane parallel to the underlying silicon substrate, so the illumination beam in a typical dark field projection system is incident on the DMD 20 degrees from the perpendicular to the plane of the silicon. The contrast ratio of a display based on such a DMD is limited by light that is diffracted from the DMD, enters the aperture of the projection system, contrast ratio is limited by ambient system's dark level and, hence, its contrast ratio. Such light is diffracted from the edges of the mirrors, torsion beams, posts, post vias, and the underlying circuit structure.

Decreasing the amount of diffracted light and thus increasing contrast ratio required a new mirror structure. The structure chosen and subsequently fabricated at Texas Instruments was first reported by Hornbeck[1] and is shown schematically in **Figure 2**.
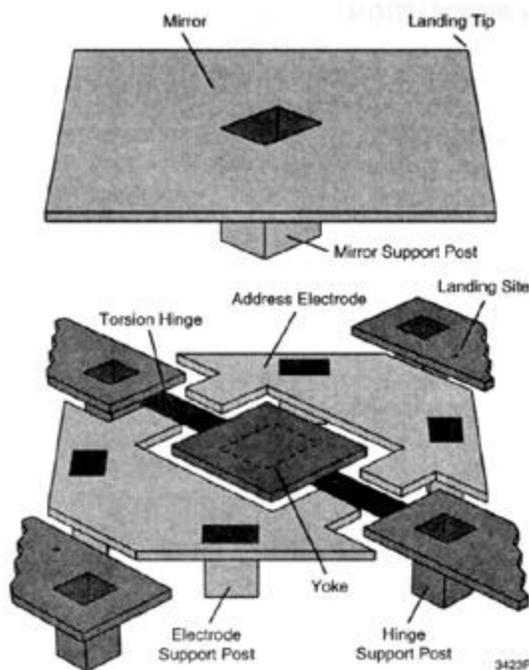

Fig. 2. A schematic drawing of the construction of a DMD mirror array that places diffractive elements under the mirror elements

A small tilting yoke, address electrodes, torsion hinges, and landing electrodes are created in the level of aluminum previously used for the mirror described above. A second sacrificial polymer layer is deposited onto this aluminum layer and vias are created from the surface of that layer to the center of each yoke. A square mirror is fabricated integral to the post formed by each via. Both sacrificial layers are removed simultaneously, leaving mirrors that tilt as before (as the yokes they ride on are tilted) but that minimize light diffracted from the underlying structure. An array of such mirrors is shown in **Figure 3**.

This mirror structure has been migrated to the 768 x 576 pixel DMD, and contrast ratios from both front and rear projection systems based on such mirrors routinely exceed 100:1. It is believed that this performance will allow the creation of commercially viable systems. With a between-mirrors gap of 1.2 micron, current DMDs with this mirror structure have an aperture ratio of 86%. The technology is expected to achieve a 0.8 micron between-mirrors gap that will result in an ultimate aperture ratio of 90%. Higher contrast

Fig. 3. A photomicrograph of a portion of a DMD mirror array fabricated through the use of the double sacrificial layer method shown in Figure 2

ratios can be achieved by limiting the aperture of the projection lens, thus discriminating preferentially in favor of reflected rather than diffracted light, but system throughput is reduced. Such tradeoffs may be justified in nondisplay imaging applications where wider dynamic ranges are required. Contrast ratios exceeding 400:1 have been observed in such systems.
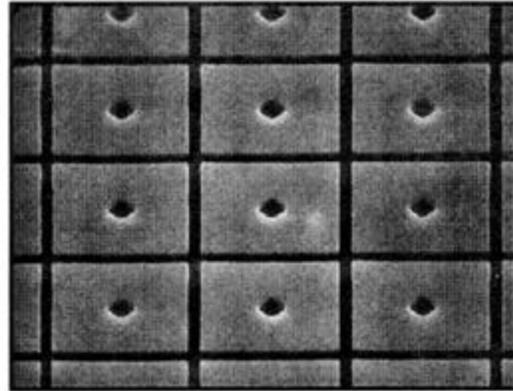
Addressing Circuitry
As discussed previously, the x-y array of DMD mirrors has been typically addressed by a congruent x-y array of SRAM cells. Gray scale in images is then achieved through pulse width modulation of the on and off (or "1" and "0") time of each mirror according to a time line, as shown in **Figure 4**. The most significant bit (MSB) from the digital intensity for each mirror is loaded into each mirror's SRAM cell at the beginning of a video frame. All mirrors remain in the MSB state for half of a frame time. The next most significant bit is then loaded and held for one-quarter of a frame time. Each less significant bit is held for a 2x shorter period until all bits

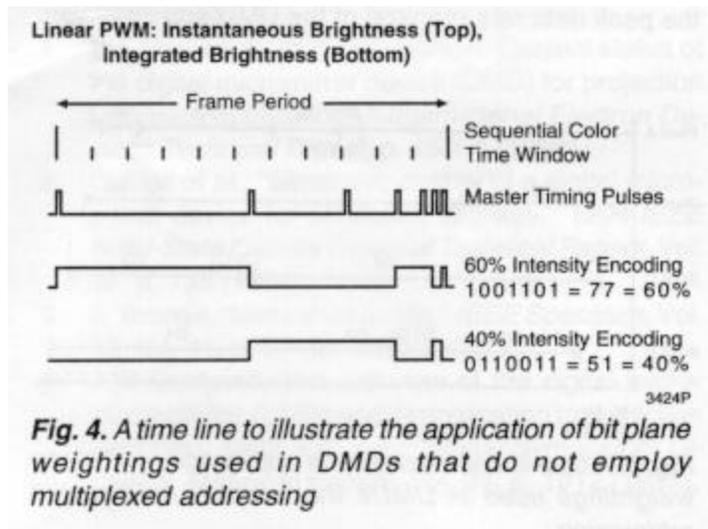**Fig. 4.** A time line to illustrate the application of bit plane weightings used in DMDs that do not employ multiplexed addressing

are shown. DMD based displays are thus operated in truly digital fashion.

Texas Instruments has identified and fabricated a new DMD addressing architecture that uses a different mode of operation and reduces device and system complexity and cost. The architecture was first reported by Tew et. al.[2] The improved device architecture was driven by two realities. First, the DMD SRAM described above must be refreshed from the least significant bit (LSB) plane of data from one frame to the MSB plane of data from the next frame during the relatively short LSB time period. This required high bandwidth DMDs and DMD drivers, even though the data rate is essentially zero throughout the 50% of the frame time represented by the MSB time period. Second, to achieve defect-free DMDs, one must fabricate defect-free SRAMs. Obviously, this is possible, but DMD manufacturability would be improved if SRAM defects could be tolerated or SRAM cell counts could be reduced dramatically below pixel counts. The new architecture takes the latter approach.

All DMD addressing schemes take advantage of a "mechanical latching" feature of the DMD. If a bias voltage in excess of the address voltage is applied to the array of DMD mirrors after the "1" or "0" address voltages are set, the mirrors will stay latched (tilted) in the selected state even if the address voltage changes. Only if the bias voltage is removed and then reapplied will the mirrors settle in the newly addressed state. This feature potentially allows multiple mirrors, provided each has a separate source of bias voltage, to be addressed by a single SRAM cell in quick succession.

Texas Instruments has constructed such a DMD with a resolution of 864 x 576 mirrors. The memory array beneath the mirrors consists of 36 rows of 864 columns. The device is divided into 16 horizontal sections (576/36 = 16) so that the memory must be loaded and transferred to segments of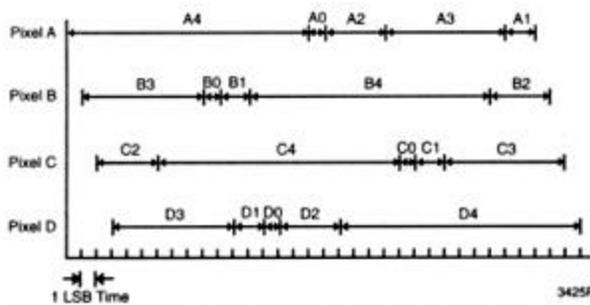 the array of mirrors 16 times to update an entire bit frame displayed by the mirrors. This addressing scheme requires a change in the simple bit plane procedure described above. **Figure 5** gives an illustration of such a changed procedure for the simplified case of a system that must display five bits of information on a DMD with four horizontal sections. The DMD sections are labeled A, B, C, and D, and the five bits are labeled 0 through 4.

Fig. 5. A time line to illustrate the application of bit plane weightings used in DMDs that employ multiplexed addressing

Note that the LSB (or any other particular bit for that matter) appears at a different time throughout the video frame in each of the four sections of the device. Also note that one section or another of the device is being updated with one bit or another almost constantly. Thus, the peak data rate required of the DMD and its drivers has been lowered essentially to the average data rate, while the DMD memory requirement has been reduced to a fraction of the pixel count. These two effects will reduce system cost through reduced bandwidth and DMD manufacturability through increased yield.

Such memory optimization, although applied here to optimize cost/performance tradeoffs, could be used to allow the DMD to approach its theoretical minimum frame

time which is in the range of 10 to 20 microseconds. This would mean that a DMD pulsewidth modulation system delivering full light efficiency could achieve over 10 bits of dynamic range.

High Resolution

A true high-resolution DMD was achieved in December 1993 with the fabrication of a 16:9 aspect ratio device of 2048 x 1152 mirror resolution. The proof-of-concept program to achieve such high-resolution DMDs is supported by the Advanced Research Projects Agency (ARPA) and the U.S. Air Force Wright Laboratory. **Figure 6** shows a 6-inch wafer, which holds 11 of the devices, and a display system electronics board with one of the high-resolution devices mounted. A projector using three of these chips/boards with dichroic beamsplitting optics has been operational since early in 1994, and its performance is reported elsewhere in these proceedings by H.C. Burstyn et al. The device was fabricated using the one SRAM cell per pixel architecture and exposed hinge and post mirror architecture described above.
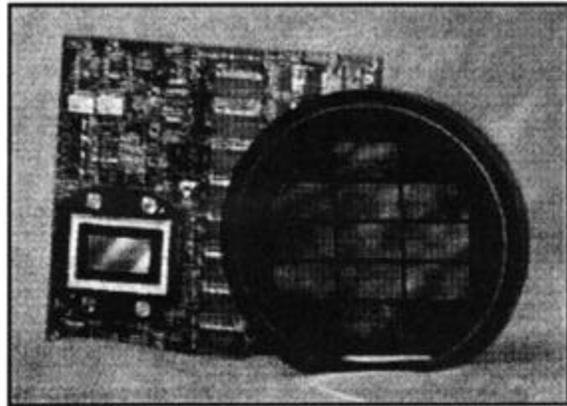

Fig. 6. A 6-inch wafer showing eleven 2048 × 1152 pixel DMD arrays and a display system electronics board with one of these high-resolution chips packaged and mounted on the board

There are several challenges to the fabrication of such high-resolution DMDs. The DMD, based as it is on semiconductor memory technology, is scaleable in many of the same ways, especially in regard to data rate and I/O width tradeoffs, as discussed above. Unfortunately, the mirrors do not scale as conveniently as do the electronics of the memory. All the devices described in this paper are based on a 171 micron square pixel, limiting the maximum number of chips per wafer. It is estimated that this cell size could be reduced to 121 microns, but image quality will most likely suffer for such small pixels and the practical pixel size minimum probably lies closer to 14 microns. Additionally, few production lithography tools are capable of printing the 2048 x 1152 array of 17 micron pixels in a single exposure so that the reticle composition techniques must be used.

Texas Instruments is at work migrating the hidden hinge and post and multiplexed addressing schemes discussed above to high-resolution DMDs. The yield improvement aspects of the multiplexed addressing scheme will be especially important for the production of cost-effective large-area DMDs.

System Considerations

As discussed previously, the DMD is an all-digital SLM. The impact on the electronic design of a display system based on such an SLM can be significant. The details of this impact are discussed elsewhere in these proceedings by R.J. Gove. However, the DMD has other, primarily nonelectronic, impacts on system design. Two such are lamp design and temporal allocation of bit weight in pulsewidth modulation.

The tilting-mirror method, which the DMD uses to modulate incident light, imposes clear restrictions on the nature of the illumination beam. The angular width of that beam must be significantly less than twice the tilt angle of the DMD's mirrors. Otherwise, the cone of reflected light in the tilted state cannot be tipped completely outside the cone of light reflected/diffracted into the nontilted direction, and on/off discrimination between these light sources will not be possible. This requirement tends to be made more difficult than it would initially appear by the size of the DMD. The DMD, at any particular pixel resolution, tends to be smaller than other practical light modulators. In general, attempts to illuminate smaller areas with light from sources of fixed physical extent lead to greater divergence in the illumination beam. Consequently, Texas Instruments believes that the identification and creation of high-intensity, long-life sources of white light with the smallest physical extent possible are key for DMD displays.

As discussed above, efforts to improve the manufacturability of the silicon addressing circuitry that underlies the DMD mirror elements have led to multiplexed memory architectures. This multiplexing, or time sharing, of memory among groups of horizontal lines of pixels within the display implies that particular bit weightings appear on different groups of lines within the display at different times during each video frame. This arrangement introduces the possibility of fixed pattern noise associated with the pattern of multiplexed lines appearing as artifacts in the displayed image. Mitigation of these artifacts through careful rearrangement of the temporal location of the bit weights requires a thorough understanding of the human perception of the artifacts. A description of the Texas Instruments methodology in this area is reported elsewhere in these proceedings by G. Deffner.

The actions taken based on the results of these studies must take into account two potential effects associated with rapid eye motion. First, the moving eye can "strobe" a large bit weight in one section of the device preferentially to another. This would result in perceived spatial intensity differences where none actually existed in the image. Second, the moving eye can sweep across the device coincidentally with the appearance of a particular small bit weight. This would result in a perceived "flash" or instantaneous temporal intensity difference where none actually existed in the image. Current work on DMD-based displays addresses the minimization of both these artifacts.

Conclusions

Projection display systems based on the digital micromirror device have been fabricated in both front and rear screen projection configurations. The image quality obtained in these systems suggests that performance on a par with or superior to other SLM technologies can be achieved. A program of technology development is ongoing at Texas Instruments to ensure that the full promise of the technology is achieved. In the last 12 months, improvements in mirror geometry have enabled increases of 33% in aperture ratio and 100% in contrast ratio. During this same period, new SRAM architectures have enabled a 6x reduction in transistor count in the memory array that drives the DMD mirrors. Additionally, a proof-of-principle demonstration of a high-resolution DMD capable of supporting most proposed high-definition standards has been achieved. All the technology advances discussed above can be migrated directly to such a high-resolution device. These advances serve as an ongoing validation of the role this unique monolithic SLM can play as an enabler of novel projection displays.

References

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