DMD 0.7 XGA 12º DDR DMD Discovery™

This data sheet is a product preview data sheet for the 0.7XGA
12º DDR DMD Discovery™.

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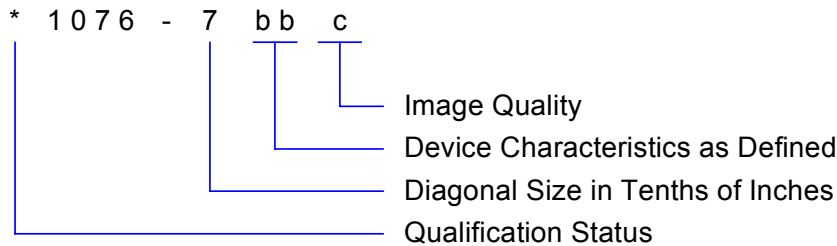
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Table 1. Product Description		
DMD Part #	**Mechanical ICD**	**Description**
*1076-729c	2503606	0.7 inch diagonal spatial light modulator of aluminum micro-mirrors. Pixel array size is 1024 X 768 in square grid pixel arrangement. Data is clocked into the DMD on both the rising and falling edges of DCLK. This is referred to as Double Data Rate (DDR). Window is optimized for visible (400-700nm) wavelengths. Pixel architecture is XB.
*1076-740c	2503606	0.7 inch diagonal spatial light modulator of aluminum micro-mirrors. Pixel array size is 1024 X 768 in square grid pixel arrangement. Data is clocked into the DMD on both the rising and falling edges of DCLK. This is referred to as Double Data Rate (DDR). Window is optimized for visible (400-700nm) wavelengths. Pixel architecture is FTP.
*1076-746c	2503606	0.7 inch diagonal spatial light modulator of aluminum micro-mirrors. Pixel array size is 1024 X 768 in square grid pixel arrangement. Data is clocked into the DMD on both the rising and falling edges of DCLK. This is referred to as Double Data Rate (DDR). Window is optimized for near infrared (900-2000nm) wavelengths. Pixel architecture is FTP.
*1076-714c	2503606	0.7 inch diagonal spatial light modulator of aluminum micro-mirrors. Pixel array size is 1024 X 768 in square grid pixel arrangement. Data is clocked into the DMD on both the rising and falling edges of DCLK. This is referred to as Double Data Rate (DDR). Process and window are optimized for near ultraviolet (350-450nm) wavelengths. Pixel architecture is FTP.

Part number description :

```
*  1 0 7 6  -  7  b b   c
```

Image Quality
Device Characteristics as Defined
Diagonal Size in Tenths of Inches
Qualification Status

Qualification status nomenclature:

X – TMX – Experimental
P – TMP – Pre-production
S – TMS – Qualified

Image quality nomenclature:

*1076-xxx8: <5 defective mirrors in active area, <2 defective mirrors in POM (Table 8), no adjacent defective mirrors, no defective mirrors stuck in the "on" position (Figure 4).

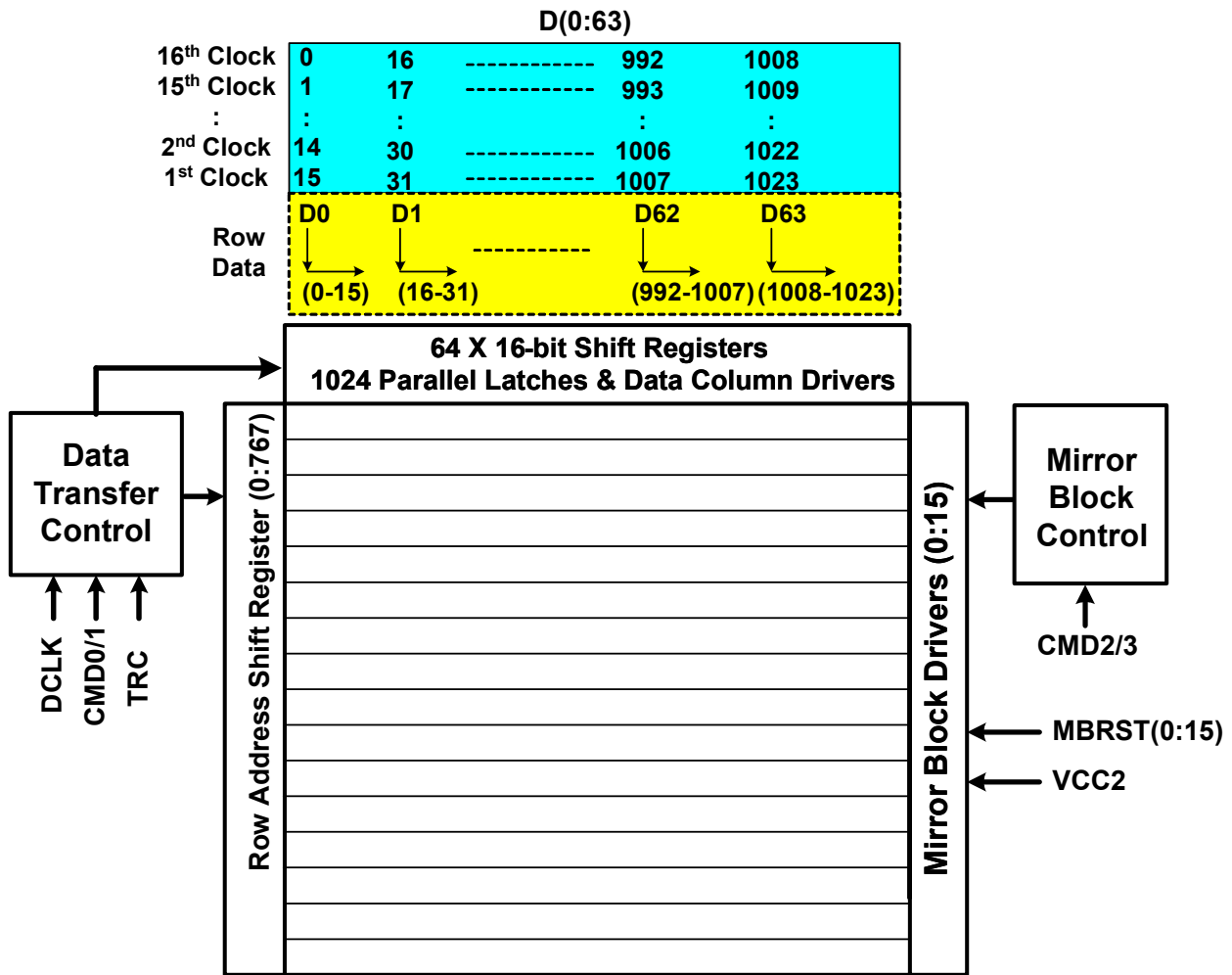*1076-xxx4: Same as –xxx8, but not screened for window blemishes.

D(0:63)

16th Clock	0	16	------------	992	1008
15th Clock	1	17	------------	993	1009
:	:	:		:	:
2nd Clock	14	30	------------	1006	1022
1st Clock	15	31	------------	1007	1023

D0   **D1**   ------------   **D62**   **D63**

Row Data

(0-15)   **(16-31)**   ------------   **(992-1007)** **(1008-1023)**

64 X 16-bit Shift Registers
1024 Parallel Latches & Data Column Drivers

Data Transfer Control

DCLK   CMD0/1   TRC

Row Address Shift Register (0:767)

Mirror Block Drivers (0:15)

Mirror Block Control

CMD2/3

MBRST(0:15)

VCC2

Figure 1 Functional Block Diagram

DMD Architecture

A functional block diagram is shown in Figure 1. Binary data is loaded one row at a time via the 64-bit data bus. The row address shift register determines which of the 768 rows is addressed. For each row the data for mirrors 15, 31, 47…1023 is loaded first and mirrors 0, 16, 32…1008 last. The DMD mirrors are grouped into 16 individually controlled blocks, with each block containing 48 rows of 1024 mirrors.

Table 2. I/O Pin Descriptions		
Pin Name	**Description**	**I/O**
D(0:63)	• Data Bus • Pin has an internal pull-down transistor circuit	I
DCLK	• Data Clock	I
CMD (0:3)	• Data and Mirror Control Signals	I
TRC	• Toggle Rate Control	I
MBRST(0:15)	• Non-logic compatible Mirror Bias/Reset inputs • Connected directly to the Array of Pixel Mirrors • Used to Hold or Release the Pixel Mirrors • Bond pads connect to an internal pull-down resistor	I
TP (65:67)	• Test points (not used in normal operation)	O
EVCC	• Pre-charge voltage during SRAM read test • Connect to VSS (GND) during normal operation	PWR
VCC2	• Mirror Electrode Stepped High Voltage	PWR
VCC	• Power Supply for CMOS logic	PWR
VSS (GND)	• Logic Ground / Common Return for all Power	PWR

Table 3. Absolute Maximum Ratings Note 1				
Parameters		**Min**	**Max**	**Units**
Logic Supply voltage : VCC	Note 2	– 0.5	4	VDC
Mirror Electrode voltage : VCC2	Note 2 Note 4	– 0.5	8	VDC
Input voltage : MBRST(0:15)	Note 2	– 28	28	V
Input voltage : other inputs	Note 2 Note 3	– 0.5	VCC + 0.3	VDC
Operating Temperature : • Reverence location 1,2, &3 in Figure 2	Note 5 Note 6	10	65	ºC
Differential Temperature : • Location 1 minus Location 3 in Figure 2 • Location 2 minus Location 3 in Figure 2			10 10	ºC ºC
Storage Temperature (non-operating) : • Reference Locations 1, 2, and 3 in Figure 2		– 40	80	ºC
Incident power (400-800nm, 25C ambient)	Note 5		45	W
Incident power density (400-800nm, 25C ambient)			5	W/mm²
Incident energy density (400-800nm, 25C ambient)			50	mJ/cm²
Operating Relative Humidity (non-condensing)		0	95	%
Storage Relative Humidity (non-condensing)		0	95	%

Note 1 : Stresses beyond those listed under "Absolute Maximum Ratings" may cause
permanent damage to the DMD. This is a stress rating only and functional operation
of the DMD at these or any other conditions beyond those indicated in the
"Recommended Operating Conditions" section of this product spec is not implied.
Exposure to absolute maximum rated conditions for extend periods may affect
device reliability.

Note 2 : All voltage values are with respect to GND (VSS).

Note 3 : Excludes reset lines MBRST(15:0)

Note 4 : It is critical to control EMI, voltage spikes, ripple and any other voltage variations that could lead
to exceeding maximum Vcc2 voltages. TI therefore recommends the installation of a zener diode on the
Vcc2 line as close as possible to the DMD. A suggested diode is the Vishay BZD27C8V2P. An
equivalent or better 8.2v zener diode capable of dissipating the full load of the DAD1000 ASIC is
recommended. TI also recommends that the user pay close attention to Electro-Static Discharge (ESD)
concerns as the DMD is an ESD Sensitive device.

**Note 5 : The DMD can be operated between 0°C and 10°C at power-up for a maximum period of 10
minutes without damage.**

Note 6:   Active Array Temperature cannot be measured directly, therefore it must be computed
analytically from measurement points on the outside of the package, the package thermal resistance, the
electrical power, and the illumination heat load. The relationship between array temperature and the
reference ceramic temperature is provided by the following equations.

$$T_{array} = T_{ceramic} + (Q_{array} \bullet (R_{array-to-ceramic})$$

$$Q_{array} = (\mathbf{0.35} \bullet P_I) + \mathbf{0.37}$$

Where,

T_{array} = computed array temperature ($^\circ$C)
$T_{ceramic}$ = measured ceramic temperature ($^\circ$C)
Q_{array} = Total DMD array power (electrical + absorbed) (watts)
$R_{array-to-ceramic}$ = DMD package thermal resistance from array to outside ceramic ($^\circ$C/watt)

P_I = incident illumination power (watts)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal power dissipation to use when calculating array temperature is **0.37 Watts**. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. The absorption constant **0.35** assumes nominal operation will all illumination power falling on the active array. For an illumination distribution of 83.7% on the active array, 11.9% on the array border, and 4.4 % on the window aperture, absorption of **0.42** should be used. A system aperture may be required to limit power incident on the package aperture since this area absorbs much more efficiently than the array.

Sample Calculation:

Incident illumination power = 20 watts
$T_{ceramic}$ = 40.0 C
Q_{array} = (**0.35** • 20) + **0.37** = 7.37 watts
T_{array} = 40.0 °C + (7.37 watts • 0.9 °C/watt) = 46.6 °C

For the maximum P_I calculation used in Table 3, $T_{ceramic}$ is calculated from $T_{ceramic}$ = $T_{ambient}$ + (Q_{array} • $R_{ceramic-to-ambient}$) assuming a liquid cooled heat sink with $R_{ceramic-to-ambient}$ = 1.5 C/watt. Substituting an air-cooled heat sink would add an additional 3-5 C/watt, thereby severely limiting the allowed incident power.

INCIDENT
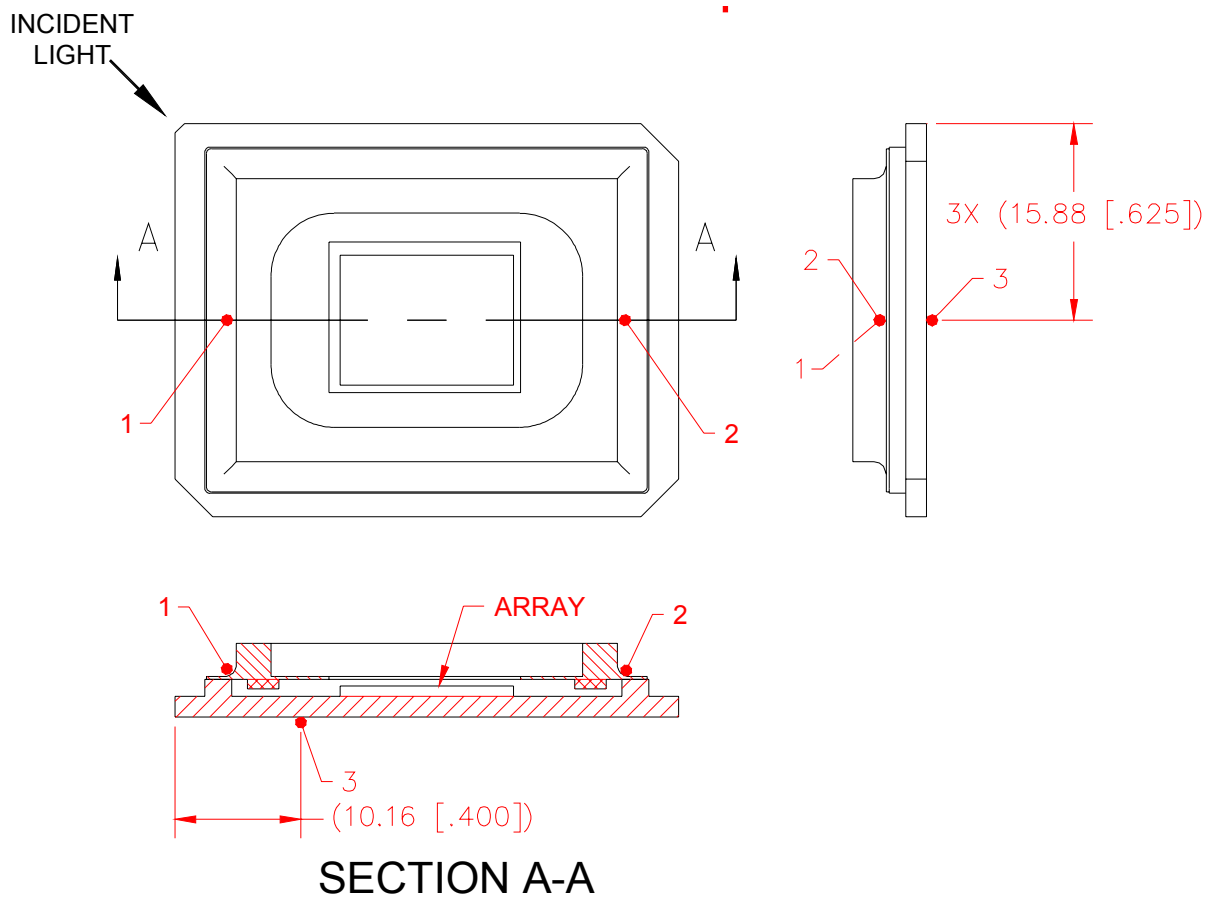LIGHT

A

A

1

2

3X (15.88 [.625])

2

3

1

1

ARRAY

2

3

(10.16 [.400])

SECTION A-A

Figure 2. Thermocouple Locations

Table 4. Recommended Operating Conditions						
Parameters			**Min**	**Nom**	**Max**	**Units**
VCC	Logic power supply voltage		3.0	3.3	3.6	V
VCC2	Mirror electrode voltage		7.25	7.5	7.75	V
V$_{MBRST}$	Mirror Bias / Reset voltage		− 27		26.5	V
V$_{IHD}$	Dynamic high level input voltage	**Note 3** **Note 4**	2.3		2.7	V
V$_{IH}$	Static high level input voltage	**Note 3**	1.7		VCC + 0.3	V
V$_{IL}$	Low level input voltage	**Note 3**	− 0.3		0.7	V
I$_{OH}$	High level output current @ Voh=2.4v				− 27	mA
I$_{OL}$	Low level output current @ Vol = 0.4v				20	mA
T$_C$	Operating case temperature	**Note 1**	25		45	^{o}C
ILL$_{UV330}$	Illumination, wavelength < 330 nm	**Note 2**			0.1	mW/cm^2
ILL$_{UV340}$	Illumination, wavelength < 340 nm	**Note 2**			1	mW/cm^2
ILL$_{UV350}$	Illumination, wavelength < 350 nm	**Note 2**			30	mW/cm^2
ILL$_{UV400}$	Illumination, wavelength < 400 nm	**Note 2**			4	W/cm^2
ILL$_{IR}$	Illumination. wavelength > 800 nm	**Note 5**			10	mW/cm^2
T$_{RST}$	Time between mirror resets on any given mirror block	**Note 6**			10	sec

Note 1 : Operating case temperature limits apply to the Array and to Locations 1, 2, & 3
referenced in Figure 2

Note 2 : DMDs optimized for 350-450nm operation (See Table 1.) must be carefully controlled in terms
of manufacturing process and illumination power spectral content. Extended use of DMDs
outside the recommended poser spectrum could result in severe lifetime degradation.

Note 3 : Simulation Conditions for V$_{IHD}$ V$_{IH}$ V$_{IL}$:
Frequency = 60 MHz
Maximum Rise/Fall Time = 2.5ns @ (20% – 80%)

Note 4 : V$_{IHD}$ min/max range is required to guarantee component set set-up & hold specifications,
using the conditions in Note 3.

Note 5 : DMDs optimized for near infrared (IR) illumination are considered experimental at this time.
While there is no known DMD damage from infrared illumination, there have been no extensive
lifetime studies above 800nm.

Note 6 : DMD mirrors are continuously reset when used in projectors. While leaving the mirrors landed
for extended periods of time causes no known damage, there have been no extensive lifetime
studies under these conditions.

DMD Marking Locations

The device marking is shown in Figure 3. The marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 3: The 2-dimensional matrix code is a alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number (example ***1076-7bbc GHXXXXX LLLLLM**). The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.
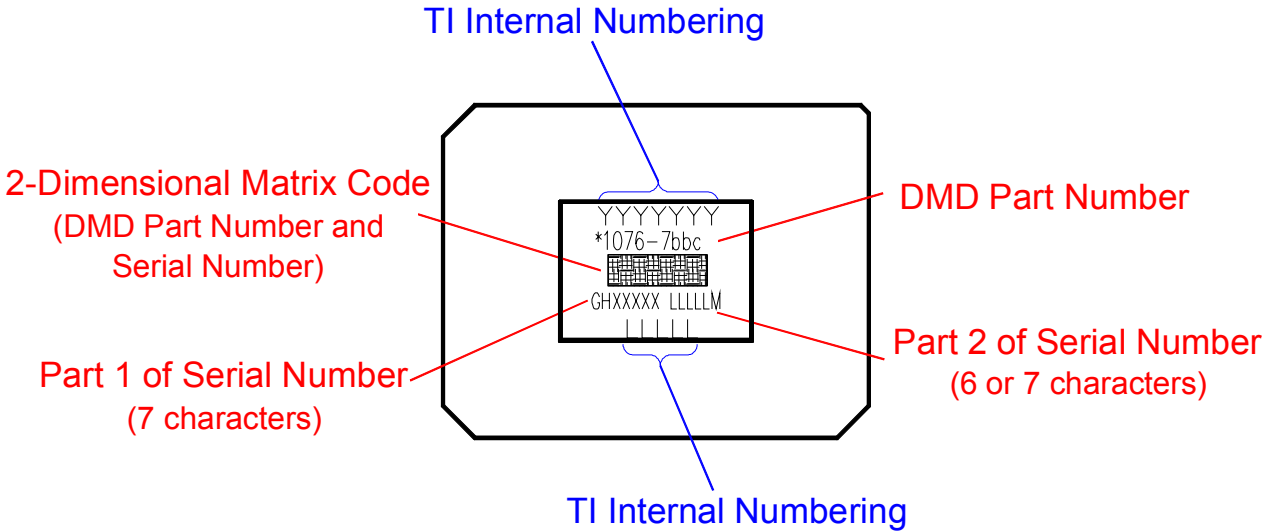
Figure 3. DMD Marking Locations

Table 5. Electrical Characteristics For Recommended Operating Conditions					
Parameters		**Test Condition**	**Min**	**Max**	**Units**
V_{OH}	High level output voltage	VCC = 3 V I_{OH} = 27 mA	2.4		V
V_{OL}	Low level output voltage	VCC = 3.6 V I_{OL} = − 20 mA		0.4	V
I_{OZ}	Output high impedance current	VCC = 3.6 V		10	uA
I_{IL}	Low level input current	VCC = 3.6 V V_I = 0 to VCC		− 5	uA
I_{IH}	High level input current	VCC = 3.6 V V_I = VCC to 0		5	uA
I_{CC}	ICC current **Note 1**	VCC = 3.6 V		400	mA
I_{CC2}	ICC2 current **Note 1**	VCC2 = 7.8 V		15	mA
	Electrical input power			1.6	W

Note 1 :

I_{CC} **and** I_{CC2} **estimates are based upon the following test conditions :**
- VCC = 3.6v
- VCC2 = 7.8v
- f = 60MHz
- temp = 27C
- alternating checkerboard pattern & inverse checkerboard pattern

Table 6. Capacitance at Recommended Operating Conditions				
Parameters		**Test Condition**	**Max**	**Units**
C_I	Input Capacitance	f = 1 MHz	10	pf
C_O	Output Capacitance	f = 1 MHz	10	pf
C_{IM}	MBRST(15:0) Input Capacitance	f = 1 MHz 1024 x 768 array all inputs interconnected	300	pf

Table 7. Critical Timing (not available for preview)		Min	Typ	Max	Units
Ts	Setup time : DATA, TRC, CMD(0:1) before rising or falling edge of DCLK				ns
Th	Hold time : DATA, TRC, CMD(0:1) after rising or falling edge of DCLK				ns
Tw	Pulse Width high or low : DCLK				ns
tr	Rise time (20% – 80%) : DCLK, DATA, TRC **Note 1**				ns
tr	Rise time (20% – 80%) : CMD (0:2) **Note 1**				ns
tf	Fall time (20% – 80%) : DCLK, DATA, TRC **Note 1**				ns
tf	Fall time (20% – 80%) : CMD (0:2) **Note 1**				ns

Note 1: Max values to be used when operated at max frequency (Tw min).

Table 8. Physical Parameters		Min	Nom	Max	Units
Number of Columns			1024		
Number of Rows			768		
Mirror (Pixel) Pitch			13.68		um
Total Width of Active Mirror Array • 1024 pixels			14.008		mm
Total Height of Active Mirror Array • 768 pixels			10.506		mm
Active Array Border **Note 1**			POM		
Active Array Border Size			6		mirrors/side

Note 1 :

The structure and qualities of the border around the active array includes a band of partially functional mirrors called the "pond of mirrors" (POM). These mirrors are structurally and/or electrically prevented from tilting toward the bright or "on" state but still require an electrical bias to tilt toward "off."

Table 9. Thermal Parameters				
Parameter	**Min**	**Nom**	**Max**	**Unit**
Thermal Resistance • Active area to case **Note 1**			0.9	°C/W

Note 1 :

The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures.

The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

Table 10. Optical Parameters				
Parameter	**Min**	**Nom**	**Max**	**Unit**
Mirror Tilt – half angle **Note 1** • Variation device to device	11	12	13	Degrees
Axis of Rotation – Lower Right to Upper Left **Figure** • Variation device to device	44	45	46	Degrees
Active Area Fill Factor (by design)		85.2		%
Mirror Metal Specular Reflectivity (420 nm – 700 nm)		89.4		%
DMD Efficiency **Note 2** (420 nm – 700 nm, visible window)		68		%
Window Refractive Index @ 545 nm – Type A		1.487		
Window Transmittance (visible window) **Note 3** measured @ 420-680 nm including AR coating	97			%
Window Flatness @ 632.8 nm spherical power / irregularity (astigmatism, etc)			4 / 2	fringes

Note 1 : Mirror Tilt

Limits on variability of mirror tilt half angle are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent non-uniformities, such as line pairing and image mottling, across the projected image. Variations in the average tilt angle between devices may result in colorimetry and system contrast variations. The specified limits represent the tolerances of the tilt angles within a device.

Note 2 : DMD Efficiency

The overall DMD efficiency includes window transmittance, active area fill factor, active area mirror specular reflectivity, and diffraction efficiency. It is defined as that percentage of light incident upon the mirror array that is specularly reflected from the mirror array. The measurement is made with all mirrors in the full on-state without electronic duty cycle effects (i.e. measure using 100% duty cycle).

Note 3 : Window Transmittance

Angle of incidence 0° - 45° at 420-680nm. Double pass system. Two AR coating surfaces at 0.5% reflectivity per AR coating.
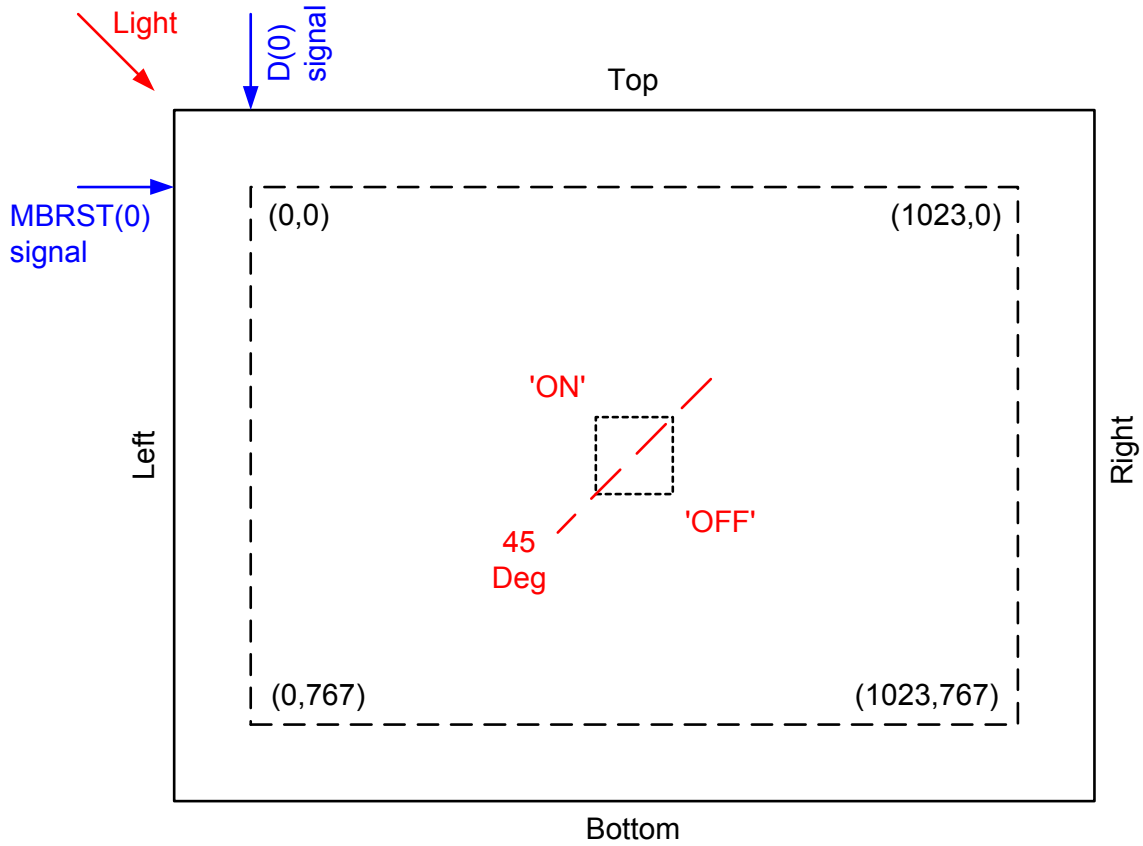

Figure 4. Mirror Tilt Axis Orientation

Table 11. Optical Interface and System Image Quality				
Parameter	Min	Nom	Max	Unit
Note 1				

Note 1 :

Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in a) through c) below :

a) Numerical Aperture and Stray Light Control. The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

b) Pupil Match. TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

c) Illumination Overfill. The active area of the device is surrounded by an aperture on the inside DMD window surface that masks undesirable structures of the DMD package from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the aperture can create artifacts from the edge of the window aperture coating and other surface anomalies that may be visible on the screen. The illumination optical system should be initially designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable..

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

The DMD 0.7XGA 12° DDR is offered in a Type A package. Package mechanical dimensions and tolerances are shown in the DMD Mechanical ICD drawing referenced in Table .

Table 12. System Interface Parameters		Min	Nom	Max	Unit
Parameter		**Min**	**Nom**	**Max**	**Unit**
Maximum Load to be Applied to the	**Figure 5**				
• Thermal Interface area				25	lbs
• Electrical Interface area				95	lbs
• Datum "A" Interface area	**Note 1**			90	lbs

Note 1 :

Combined loads of the thermal and electrical interface areas in excess of the Datum "A" load shall be evenly distributed outside the Datum "A" area (95 + 25 – Datum "A"). Refer to Figure 5 for package interface load diagrams.
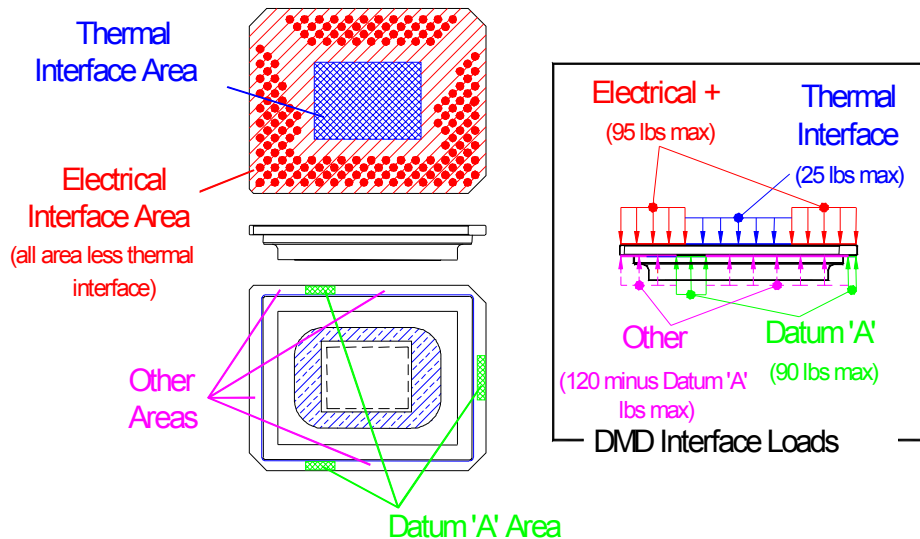
Thermal interface and Datum 'A' areas defined in the Mechanical ICD.

Figure 5. System Interface Loads

Table 13. Pad Coordinates vs Signal Name			
(not available for preview)			
PAD #	**SIGNAL NAME**	**PAD #**	**SIGNAL NAME**

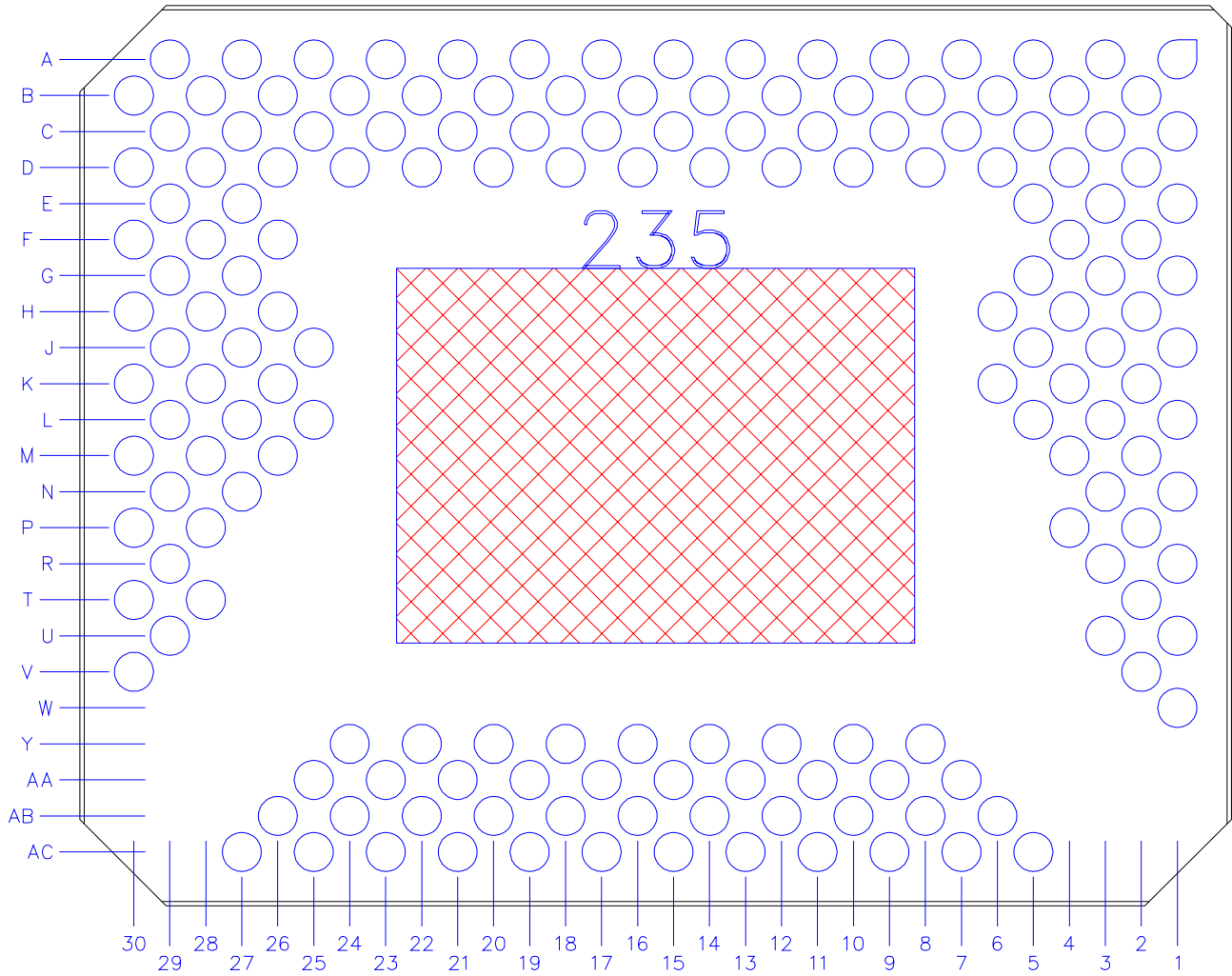|	

Figure 6. Package Back Pads

Electrostatic Discharge Immunity

Caution

MBRST(0:15) ESD input protection is limited to charge sharing between the ESD source and the intrinsic capacitance of the signal.

Please see Note 4 of Table 3 on VCC2 sensitivity.

Notes on Handling

All CMOS devices require proper ESD handling procedures. Refer to Drawing # 4144804 (DMD Handling & Cleaning Procedure) for static charge prevention, dust and dirt protection.