Implementation of a Pipelined Optoelectronic Processor: OCULAR-II

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Introduction

Recent advances in technologies such as modulators, vertical cavity surface-emitting laser (VCSEL) arrays, optoelectronic VLSI, and micro-optics has allowed the construction of parallel optoelectronic computing systems utilising the high bandwidth, high density and global nature of optical communication paths to overcome some of the limitations of conventional electronic connections interconnections. Global high-bandwidth optical connections among processors are suitable for applications such as sorting, FFTs, signal processing, matrix computations and image processing.

We are constructing a general purpose optoelectronic processor capable of performing many of these tasks in which the processing elements (PEs) are programmable and the optical interconnections are dynamically reconfigurable. Our system is based on the pipelined architecture shown in Fig. 1 [1]. Two-dimensional arrays of optoelectronic PEs are connected via parallel optical connection paths using VCSEL arrays and photodetector (PD) arrays. Local neighbourhood connections are provided electrically on the PE chip; global interconnectivity is achieved by the optical links which are dynamically reconfigurable. This allows the machine to use an interconnection topology that is best suited to the algorithm being performed.

Ishikawa and McArdle described an implementation of this architecture known as Optoelectronic Computer Using Laser Arrays with Reconfiguration (OCULAR) [2] in which a single layer of the pipeline is arranged in a feedback configuration. McArdle *et al.* also described the design of a fully pipelined version of this architecture [3] and here we describe the experimental realisation of a system based on it which is known as OCULAR-II.

OCULAR-II Implementation

As an intermediate goal of realising the fully integrated pipelined system shown in Fig. 1. we have designed OCULAR-II, which is a two-layer pipelined prototype in which the PD array, PE array and VCSEL array are implemented as separate components. Fig. 2. shows a schematic diagram of the system. There are two processing layers in diagram, each being composed of a PD array for optical input, a VCSEL laser-diode array for optical output, and an array of electronic processing elements. The system has 8x8 channels connected in a fully parallel fashion. Each processing element module is connected to a control computer via a dual-port RAM into which instructions can be downloaded. The outputs from the PEs on the left are conveyed to the input of the PEs on the right via an optical interconnection unit. The specifications of the main components are shown in Table I.

Processing Element Module The PE array is configured as a general purpose 8x8 SIMD array. Each PE contains a 24 bit memory and a programmable arithmetic logic unit (ALU) for performing bit-serial operations. The design was described in detail in [1] and [2].

Photodetector Module The optical input is provided from a 8x8 PIN photodetector array and amplifier array. These devices provide 64 direct outputs for interfacing to the inputs of the 64 PEs. The speed of our initial demonstrator systems is not crucial, since the clock rate of the FPGA PE array is limited to around 12 MHz. Some specifications are given in Table I.

Optical Interconnection Module This consists of a 4-f imaging system in a reflection configuration. A phase modulating spatial light modulator (SLM) is placed at the Fourier plane and displays computer generated holograms (CGH) for changing the interconnection topology. To make

the system as compact as possible, the optical path is folded several times by mirrors and a prism. A plan view of the module is shown in Fig. 3 and it is described in more detail in [4].

PE Module		**PD Module**	
Type	custom designed FPGA	Type	PIN photodiode array
Array Size	8x8 PEs	Array Size	8x8
Architecture	SIMD processor array	Device pitch	250 μm
Functionality	Programmable bit serial ALU	Amplifiers	CMOS TZ amp and comparator, or bipolar TZ amp
Inputs	64 parallel inputs	Configuration	CMOS: integrated in same die Bipolar: 4x16 ch. TZ amp mounted around PIN die and wire bonded
Addressing	SIMD type, 6 bit instruction word, 5 bit address word	Detector size	Circular 110 μm diameter
Outputs	64 parallel outputs	Bandwidth	PD: >1 GhZ TZ amp: 20-35 MHz
Interconnection	Local 4-neighbours	Responsivity	0.5 A/W
Clock rate	~50 MHz	Package	PGA Package
Interface	To PC via dual-port RAM	Peak reponse	800 nm
VCSEL Module		**Optical Interconnection Module**	
Array Size	8x8	Type	Optical addressed nematic PAL-SLM
Device pitch	250 μm	Modulation	Phase only (>2π)
Wavelength	840 ± 15 nm	Resolution	PAL-SLM 50 lp/mm, SLA 10 lp/mm
Output power	~ 4.0 mW at 15 mA drive current	Frame rate	50-70 Hz (limited by LCTV)
Threshold current	7 ± 1 mA typical	Addressing	Addressed by liquid crystal TV
Output	Multimode (spatial and temporal)	Coupling	SELFOC lens array (SLA)
Drivers	4 x 16 channel driver ICs on PCB board	Fourier transform lens	360-440 mm zoom Fourier transform lens (4 elements)

Table I. Specifications of the main devices

Future Work and Summary

OCULAR-II is in intermediate step to realising a fully integrated, pipelined parallel processing system. It is a demonstration system which allows us to investigate issues such as architectures, interfacing and control, optical interconnection, reconfigurable topologies, packaging, alignment, and applications, and algorithms [5]. Although the processing layers are implemented as separate components, the specifications and dimensions of the CMOS PE array, VCSEL array, and PD array are very similar to those that would be achieved if complete integration was possible.

Our laboratory is actively developing CMOS processing circuits in which the PEs and PDs are integrated. We are developing a full-custom VLSI chip using a 0.35 μm process which integrates 64x64 PD+PEs, each in a 150x150 μm^2 area. Further work still needs to be done on integrating the light sources (VCSELs) with these devices to form completely integrated units with input, output, and processing in parallel.

We are also designing more compact optoelectronic systems in which the optoelectronic modules are implemented using multichip modules which contain the PE arrays, VCSEL arrays, PD arrays, drivers, and amplifiers, rather than individually packaged devices. Other integration techniques such as solder-bump flip chip bonding or monolithic integration are also promising technologies for our systems.

References

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3. N. McArdle, *et al.*, *Optics in Computing '98*, Proc. SPIE, **3490**, pp302-305 (1998).
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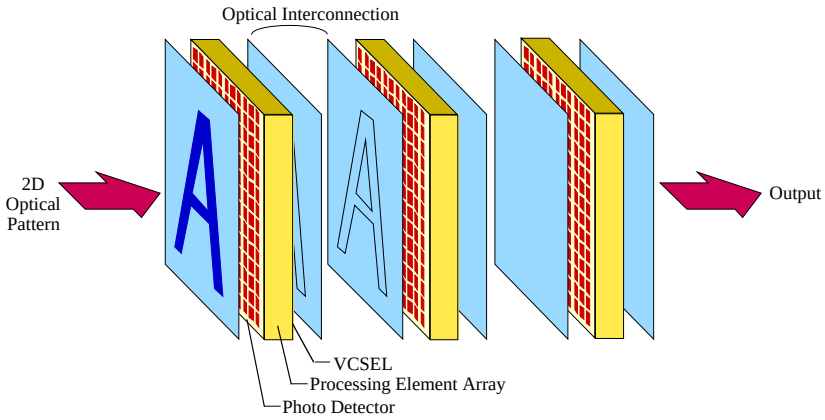

Fig. 1. Conceptual drawing of free-space interconnected pipelined architecture.

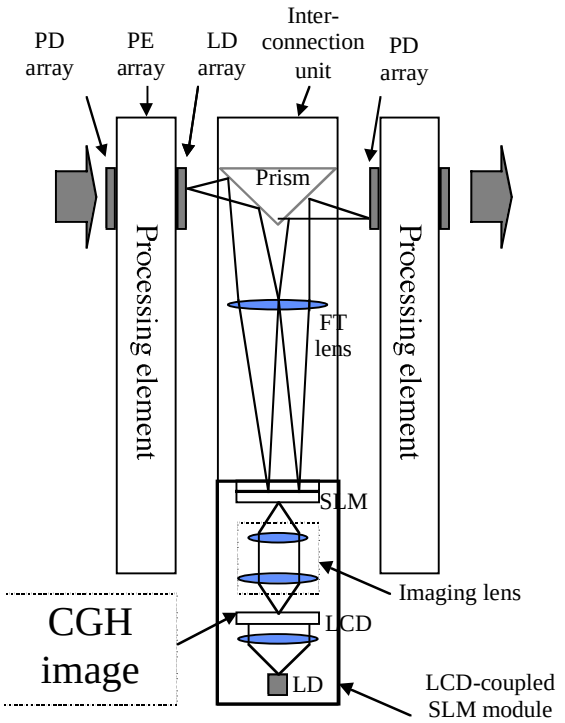

Fig. 2. Implementation of two layers of the pipeline.

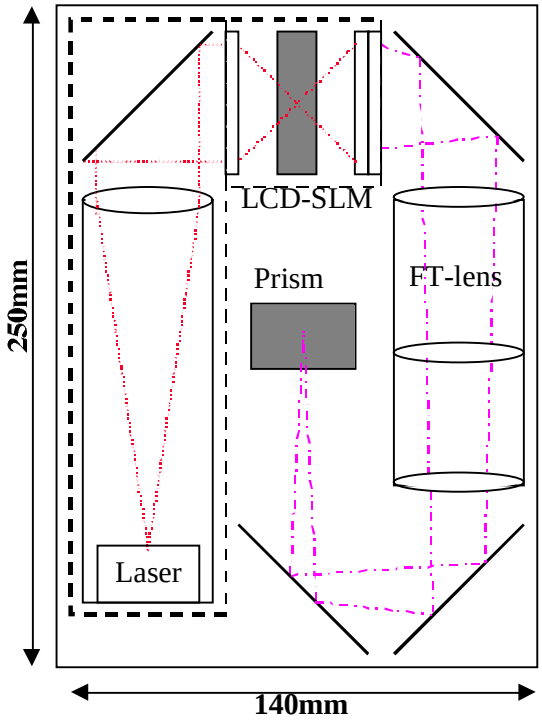

Fig. 3. Plan view of the interconnection unit

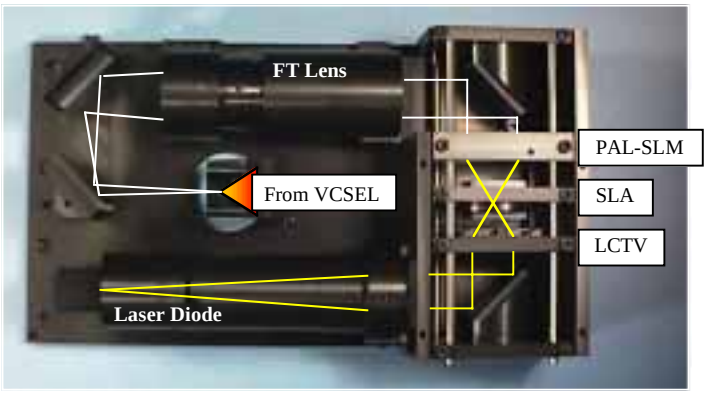

Fig. 4. Photograph of the optical interconnection unit

Fig. 5. Photograph of the PD board showing the PD array