

P-9: TV Display Applications by an Advanced Multi-Media Display Processor (AMDP2)

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Abstract

The AMDP2 provides various features for current television system such as frame synchronization, de-interlace, still image display, multiple pictures display and so on. AMDP2 is a programmable device which allows customers to realize their signal processing algorithm. By using AMDP2 and its capabilities, various video format signals can be converted to specific screen format and displayed on any monitor, including TV, PC, LCD, PDP and DLP.

Introduction

1.1. Background

At the recent digital broadcasting, some programs are transmitted with different scanning method, number of scan-lines and pixels. Therefore, conventional TV may not be able to display the even decoded signal. Regarding the display monitor, there are various types of displays in the market such as conventional TV, aspect ratio with 16:9 so called wide-TV, high-definition TV, plasma display panel (PDP) and so on. So it is required to convert various formats for particular monitor to fit in.

The followings were the design objectives for the development of the system;

- Different signal processing can be implemented by witching the software on the same hardware.
- Development turn around time (TAT) should be minimized.
- The system should be easy to modify.
- Mass production should be possible with lower price.

1.2. TV Market Environment

In the current TV market, ASIC solutions are employed for the most of digital video processing and format conversion. But our Scan-line Video Processor (SVP) is used for some video applications as non-ASIC solution. If ASIC solution is employed for digital broadcasting, the total gate size will be increased in proportion to the number of formats, and development cost and TAT are also increased. MCU and DSP are also programmable devices for signal processing, but it is not fast enough for real-time video signal processing. An SVP is only programmable device for video application. The AMDP2 consists of the SVP, multiple pictures display function, a timing controller and an SDRAM interface to reduce the total system cost. The processing speed of the SVP on the AMDP2 has been increased to 140MHz. By using AMDP2's programmability, user can implement their original signal processing algorithm on the AMDP2, and realize various applications by switching its program on the same hardware configuration.

This paper outlines the TV display applications using an AMDP2.

AMDP2 architecture

(See "Figure 1. AMDP2 block diagram")

The AMDP2 consists of various blocks; an SVP for signal processing, an SDRAM Interface for controlling data transfer between the AMDP2 and an external SDRAM, a Video Input (Output) Unit for transfer the input (Output) video data stream to (from) internal data path, a Video Statistics Analyzer for extracting statistics value, a Timing Control Unit for internal timing generation and Data Network for controlling the internal data path. All blocks in the AMDP2 operate the functions according to the register settings and the programs. The SVP program and register settings are downloaded from an external program ROM or the universal serial data interface. The package is a Micro Star BGA with 257pins.

1.3. SVP

(See "Figure 2. SVP block diagram" and "Figure 3. SVP-PE operation")

The AMDP2 has the SVP for signal processing. The SVP has 1288 Processing Elements (PE's), and executes signal processing algorithm as a parallel processing manner. The SVP is a Single Instruction Stream, Multiple Data Stream (SIMD) processor which performs real-time video processing. PE's in the SVP are aligned on one dimension. Each PE corresponds to a pixel on a horizontal scan-line. One PE consists of a 1-bit ALU, four working registers (WRA, WRB, WRC and WRM), a 416-bit register file and a 11-bit PE number ROM (PENO-ROM). The PENO-ROM is used to identify individual PE which may be required on algorithms differed PE-by-PE. The SVP executes the video processing such as the horizontal/vertical filtering, scaling, edge enhancement, color phase adjustment and so on. The processor runs with 140MHz (Max). The computation ability is 20.04GOPS (140MHz X

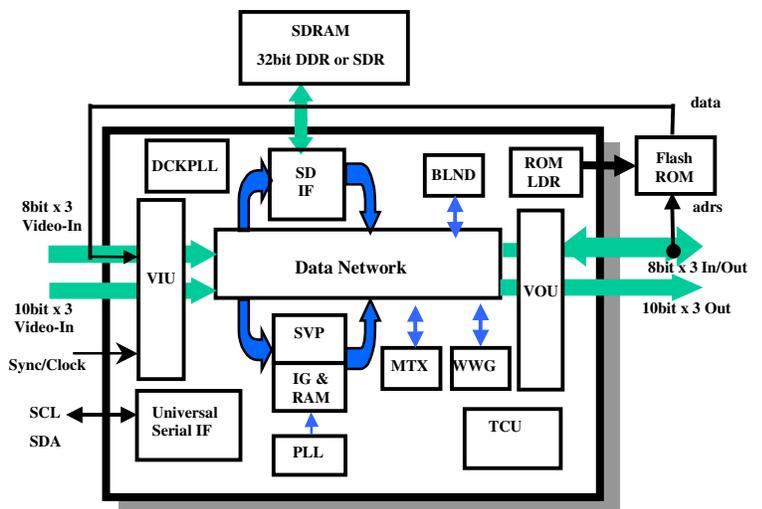


Figure 1. AMDP2 block diagram

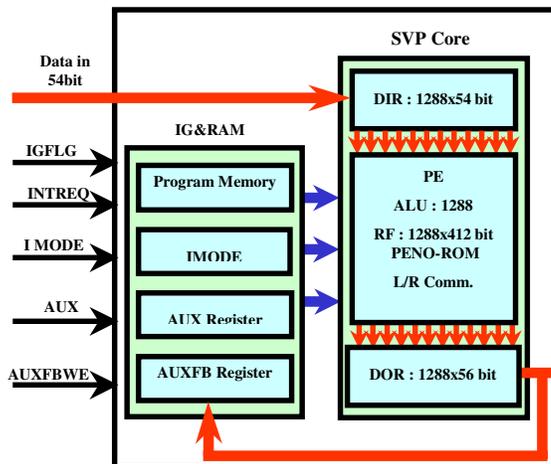


Figure 2. SVP block diagram

1288PE/9clk) for 8-bit addition and 2.47GOPS (140MHz X 1288PE/73clk) for 8-bit multiplication. This SVP has 54-bit input and 56-bit output.

1.4. Data Network

Data Network (DTN) provides flexible data path connection among Input Line-Memories (LMEM) in VIU, Output LMEM in VOU, SVP, SD-IF, Matrix (MTX), Double Window Generator (WWG) and Blending (BLND). Up to eight Data Packets (DP) are allowed during a horizontal video period to multiplex up to eight different data on each data path for multiple and complicated video processing. Operating clock can be selected either from Processor clock (PCK) for SVP or internal data clock (DCK). MTX provides a color space conversion, or three cubic curves. Two sets of calculating coefficients are provided by register setting to allow two different matrix calculation and polynomial calculations. BLND blends two video streams to get a single transparent superimposed picture. WWG generates a single superimposed picture from two video sources.

1.5. Video Input Unit (VIU)

VIU is located at the AMDP2 input portion and has three 10-bit and three 8-bit video data input ports for multiple video processing. VIU consists of Bit Parallel Decoder, Video Input Filter (VIF), Input Line-Memories (LMEM) and Input Sync Generator (SYGIN). Bit Parallel Decoder converts SMPTE-125/267/260/274/296 (or CCIR-656) to 4:2:2 data stream. VIF decimates or inserts pixels on input video data stream to fit the number of pixels with PE on SVP. Input LMEM isolate input video clock system from internal clock system for SVP and SD-IF for flexible operation. SYGIN generates various synchronization timing for AMDP2 operation from HSYNC/VSYN input.

1.6. Video Output Unit (VOU)

VOU consists of three 10-bit video output ports and three video input/output ports for multiple video processing. Two 4:2:2 to SMPTE-125/267 (or CCIR-656) encoders allow data stream output. VOU has Output LMEM and Output Sync Generator (SYGOUT) as same as the VIU. The VOU also has capability to add the blanking data according to timing signal from the TCU. The blanking level is defined by the register setting in the VOU.

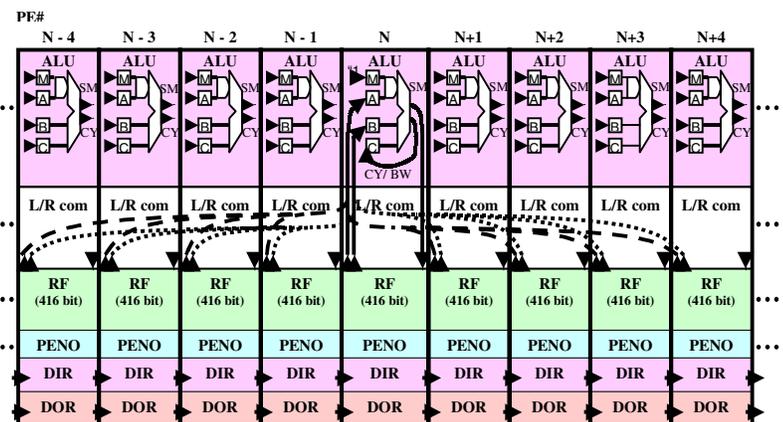


Figure 3. SVP-PE operation

1.7. SDRAM-Interface (SD-IF)

The SD-IF consists of an SDRAM controller and data buffers to store and retrieve video data to/from external SDRAM with ultra high speed. Based on the timing signal from the TCU, the SD-IF provides Write/Read timings and addresses to the external SDRAM. When 8-bit data is input to the SD-IF, this data is converted to 32-bit width data stream, then written to the SDRAM. To read the data from the SDRAM, opposite manner is performed by the SD-IF. The SD-IF divides the SDRAM memory area up to six logically definable areas (four Delay/Async area and two Still area). For the frame synchronization, asynchronous input data (sub-picture) is written into the asynchronous area on the SDRAM. Then the data is read by main-picture timing. In the still image area, the data stays unchanged as still image until new data is written in this area. The delay area is used to generate various delayed signals such as field delay signals. Four SDRAM Input (Output) buffers; SDIA, SDIB, SDIC and SDID (SDOA, SDOB, SDOC and SDOD) for introducing (delivering) up to four different video data from (to) Input (Output) LMEM, MTX, BLND, WWG and SVP simultaneously. By controlling the address pointer of each block, the data scaling can be performed. The SDRAM data transfer speed is 140MHz max. with 8-burst transfer mode. The SD-IF supports single 32-bit data width DDR-SDRMA or SDR-SDRAM.

1.8. Video Statistics Analyzer (VSA)

This VSA can extract the maximum, minimum, average value and histogram from two designated areas on a display field area. There are two modes for histogram extraction; fixed 8-bin and adaptive 4-bin between maximum and minimum on the previous field. These extracted values are introduced to the SVP as parameters for signal processing. Therefore data adaptive signal processing can be realized with this capability.

1.9. Timing Control Unit (TCU)

The Timing Control Unit (TCU) generates internal timing signals from external clock and H/V-synchronization pulse, and supplies to Input LMEM, Output LMEM, MTX, BLND, WWG, SVP, SD-IF and DTN as data write timing signal, data read timing signal and so on. TCU also generates horizontal/vertical/field-ID timing signals and interrupt request (INTREQ) for signal processing on the SVP. All timing signals are defined by the register settings in the TCU.

The register settings are loaded from the external program ROM or the universal serial data interface. The TCU gets four external clock and H/V-sync inputs, and can handle up to three asynchronous video signals.

AMDP2 Application

(See “Figure 4. AMDP2 application block diagram”)

Using a single AMDP2, we have developed four application programs; “Motion adaptive de-interlacing”, “Double window mode display”, “Channel search mode display” and “Non-linear horizontal scaling (so called Panorama)”. All input pictures are converted from interlace to progressive scan (de-interlacing). These are major TV applications in the current sophisticated TV, and are realized on the same hardware by switching the application program.

Two signal sources are introduced to the system; DVD player for the main-picture and LD player for the sub-picture. Both pictures are converted from analog composite to two 8-bit data, Y/CrCb in 4:2:2 format, by an NTSC decoder TVP5020. Then these two asynchronous video data are introduced to the AMDP2 at 14.3MHz. On the AMDP2, these data are computed for scaling and de-interlacing, and converted to R/G/B data from Y/CrCb. Then three 8-bit data, R/G/B, are output from the AMDP2 with 28.6MHz to a TV monitor through external D/A-converter.

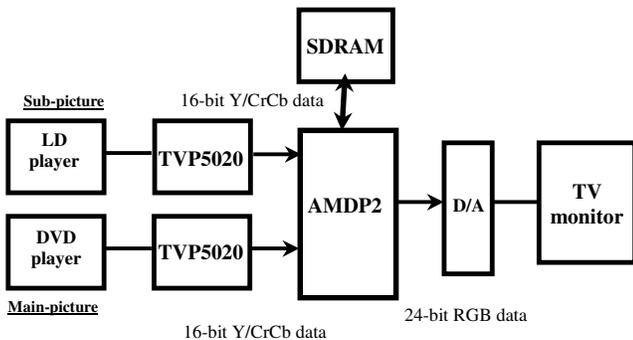


Figure 4. AMDP2 application block diagram

1.10. Motion Adaptive De-interlacing

(See “Figure 5. Motion adaptive de-interlacing block diagram”)

Firstly, single input video data is written directly to the SDRAM

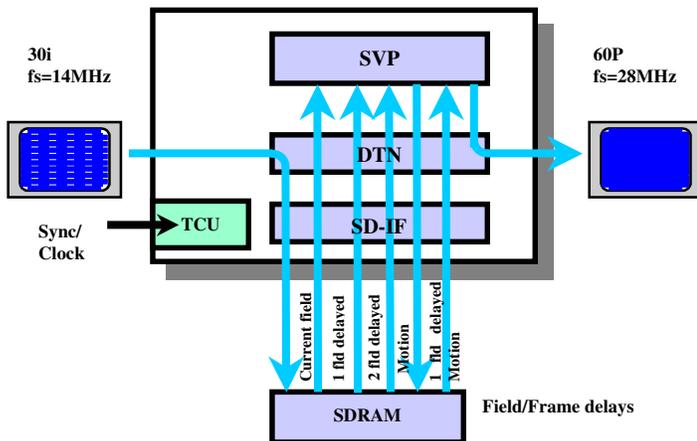


Figure 5. Motion adaptive de-interlacing block diagram

delay area. Then several field-delayed signals, such as current, 1-field delay and 2-field delay, are read from the SDRAM and provided to the SVP. From these delayed data, the SVP extracts the motion information and also performs two interpolation methods for motion and still image by pixel basis. Then SVP selects the appropriate result data according to motion information, then output it as motion adaptive de-interlacing. Using an SDRAM, instead of using FIFO memories, reduces system cost and provides more memory capacity for complex signal processing.

1.11. Double Window Mode Display

(See “Figure 6. Double window mode block diagram”)

In this application, two asynchronous video signals, main- and sub-picture, are input to the AMDP2. The main-picture is lead to the SVP directly, and sub-picture is written into the SDRAM asynchronous area, then read out that data to the SVP with main-picture timing for frame synchronization. These two synchronized data are introduced to the SVP, and horizontal and vertical high frequency component is removed for decimation and also de-interlacing is performed, then output to the SDRAM delay area with 28.6MHz. The data are written into the SDRAM delay area for the horizontal and vertical picture decimation. The progressive-scanned shrunk pictures are read from the SDRAM and displayed as single screen as “Double window mode”. One of the picture sizes can be changed from 1/2 to 2/3 while another picture size changed from 1/2 to 1/3 with smooth action. To realize smooth action, only two AMDP2 programs (both pictures 1/2, and one 2/3 with another 1/3) are required to develop by user, and the AMDP2 Utility software “Codegen” automatically creates specified number of intermediate states. The smooth action is realized by downloading the intermediate states sequentially. This AMDP2 “Codegen’s” function reduces application development TAT.

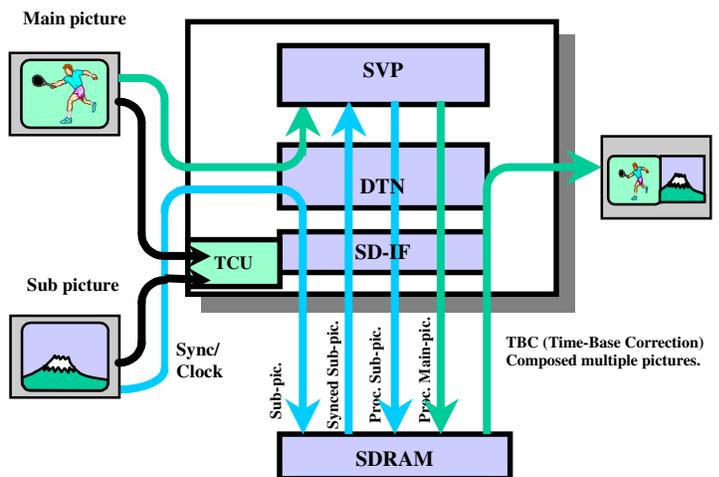


Figure 6. Double window mode block diagram

1.12. Channel Search Mode Display

(See “Figure 7. Channel search mode display example”)

As well as the “Double window mode” application, two asynchronous video signals, main- and sub-picture are input to the AMDP2, then frame synchronization is executed for sub-picture with the SDRAM asynchronous area. The main- and sub-picture pass the low-pass filter and are executed de-interlacing on the SVP. The main-picture is decimated to 1/2 size and the sub-picture is

decimated to 1/4 size. The main-picture is written into the SDRAM delay area, and the sub-picture is written into the still image area. When the sub-picture is switched to other broadcasting channel, the write address of the SDRAM still image area is shifted to display new channel on a shifted location, and the previous channel sub-picture is stayed as still image. A multi-picture display on a single screen is realized by reading the whole still image area. As described on previous section, only two programs for the first and the last position of the sub-picture are created, and the AMDP2 “Codegen” automatically created intermediate positions. “Figure 7.” shows an example of channel search mode display. The picture alignment can be changed according to the program.

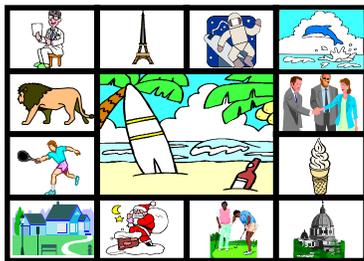


Figure 7. Channel search mode display example

1.13. Non-linear Horizontal Scaling (Panorama)

(See “Figure 8. Non-linear horizontal scaling block diagram”, and “Figure 9. Scaling processing”)

Recently non-linear horizontal scaling (so called PANORAMA) function is required for 16:9 aspect ratio display monitors, especially for flat display panels. This function naturally fits a 4:3 aspect ratio picture on a 16:9 display. In this application, single picture is input to AMDP2. Then de-interlacing and non-linear scaling are performed. As the Panorama processing, we implemented forth degree polynomial equation with using the content of PENO-ROM, and calculated the pixel shifting number for scaling during vertical blanking period. Then pixel shifting and interpolation is performed during active video period. We

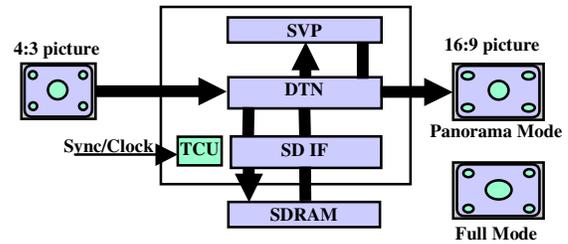


Figure 8. Non-linear horizontal scaling block diagram

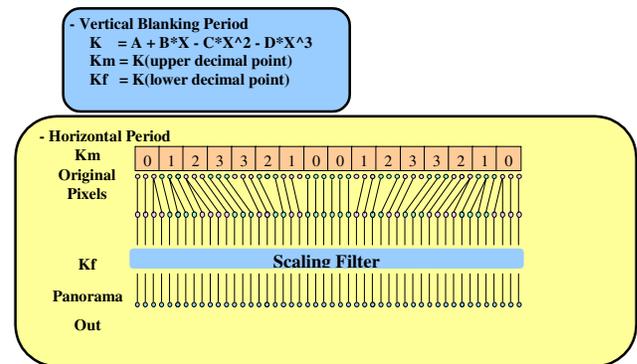


Figure 9. Scaling Processing

employed cubic interpolation filter for Y data and bi-linear for Cr/Cb data. Since SVP is a programmable processor, we chose appropriate values for the constants of equation to get a expected Panorama curve.

Conclusion

We have developed the TV display applications using a programmable display processor AMDP2. By switching its software, function change, picture quality improvement and input/output signal format conversions are realized. This signal processing capability can be used not only TV, but any display applications in PC and Monitor market.