DATA MODUL
DISPLAY AND SYSTEM SOLUTIONS

Specification for MGLS19264

MGLS19264-HT-LED04 (MGLS19264-25)

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VARITRONIX LIMITED

LCM Design Engineering

PRELIMINARY SPECIFICATION

FOR

LCD MODULE TYPE

ITEM NO.: MGLS19264-25

MGLS19264-HT-LED04

(DOCUMENT REVISION 0.0)

DEPARTMENT	NAME	SIGNATURE	EFFECTIVE DATE
PREPARED BY	PHILIP CHENG		2001.06.01
APPROVED BY	CYRUS CHEUNG		2001.06.01

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Preliminary Specification
of
LCD Module Type
ITEM NO.: MGLS19264-25
MGLS19264-HT-LED04

1. General Description

- 192 x 64 Dots STN Positive Green-Yellow Transflective Dot Matrix LCD module.
- Viewing Angle: 6 o'clock direction.
- Driving duty: 1/64 duty, 1/9 bias.
- 'HITACHI' HD61202 (flat pack form) or equivalent dot matrix LCD segment drivers.
- 'HITACHI' HD61203 (flat pack form) or equivalent dot matrix LCD common driver.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	100.0(W) x 60.0(H) x 15.0(D)MAX.	mm
Effective viewing area	84.0(W) x 31.0(H)	mm
Active area	78.67(W) x 26.19(H)	mm
Display format	192(Horizontal) x 64 (Vertical)	dots
Dot size	0.36(W) x 0.36(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch for characters	0.41(W) x 0.41(H)	mm
Weight	TBD	gram

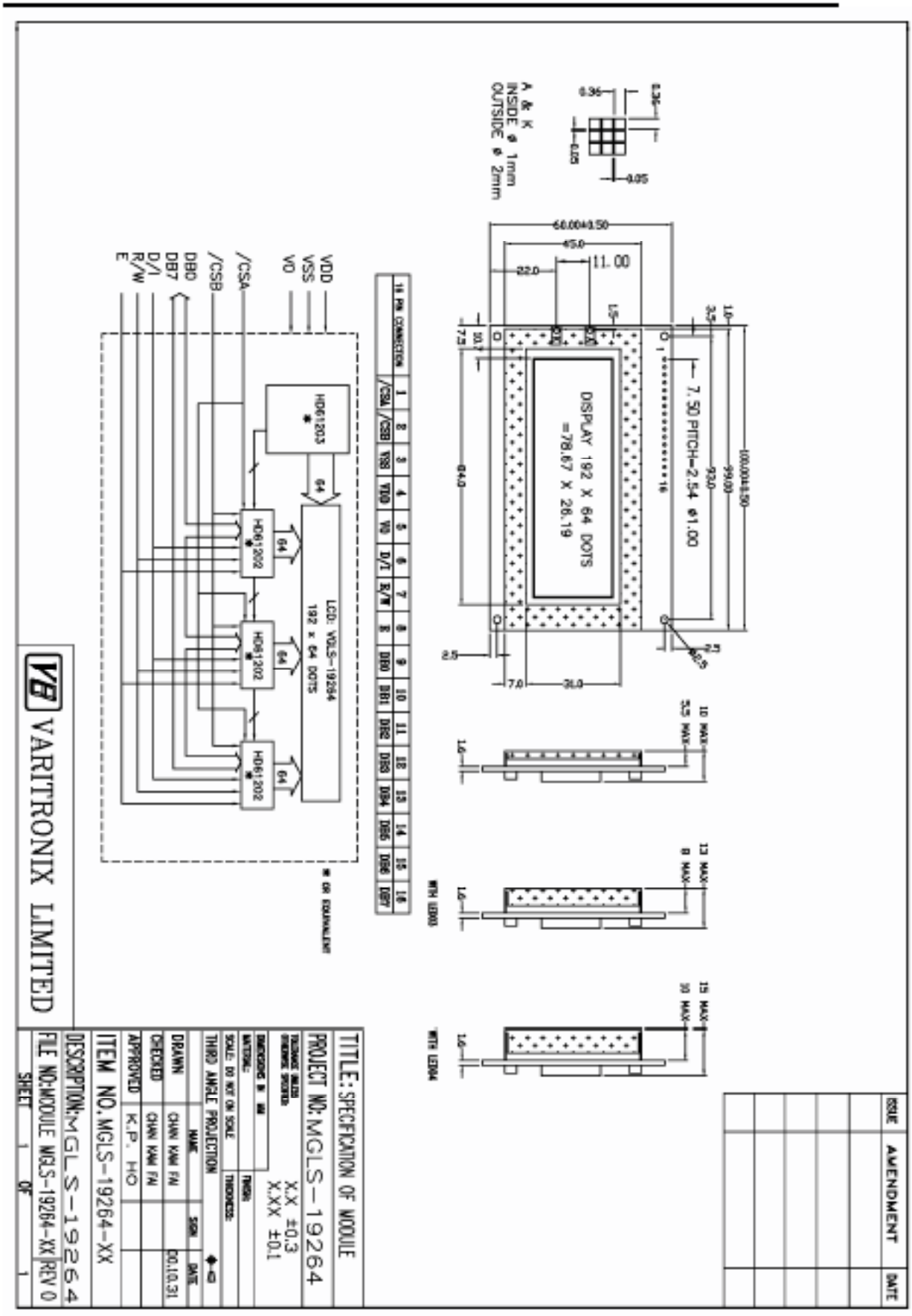

FIGURE 1: An outline drawing

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = 25 °C)

Table 2

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VDD - V_O	-0.3	+17.0	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:
The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltage values are referenced to Vss = 0V.

3.2 Environmental Condition

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	/CSA	Chip selection A : In order to interface data for input or output.
2	/CSB	Chip selection B : In order to interface data for input or output.
3	VSS	Ground
4	VDD	Power supply for logic (+5V)
5	V_O	Power supply for LCD driver
6	D/I	Data or instruction select input D/I=High : Display RAM data on D0-D7. D/I=Low : Display instruction data on D0-D7.
7	R/W	Read/Write control signal input pin. R/W = High : CPU to read data appearing at DB0 to DB7. R/W = Low : Data of DB0 to DB7 is latched at the falling edge of E.
8	E	Chip Enable. E = High: Read data appears at DB0 to DB7 as E is at high level. E = Low : Write data of DB0 to DB7 is latched at the fall of E.
9	DB0	Data input/output (LSB)
10	DB1	Data input/output
11	DB2	Data input/output
12	DB3	Data input/output
13	DB4	Data input/output
14	DB5	Data input/output
15	DB6	Data input/output
16	DB7	Data input/output (MSB)
A	LED(+)	Anode of backlight
K	LED(-)	Cathode of backlight

4.2 Electrical characteristics at Ta = 20 °C, VDD = 5V±5%, VSS = 0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (Logic)	VDD - VSS		4.75	5.0	5.25	V	
Supply voltage (LCD)	VDD -V_0	VDD =5V	-	TBD	-	V	Note 1
High Input signal voltage	V_{IH}		2.0	-	VDD	V	Note 2
Low Input signal voltage	V_{IL}		0	-	0.8	V	Note 2
Supply Current (Logic & LCD)	I_{DD}	VDD =5V	-	TBD	-	mA	
Supply Current (LCD)	Io		-	TBD	-	mA	Note 1
Supply voltage of yellow-green LED04 backlight.	V_{LED04}	Forward current =180mA Number of LED chips =36	3.8	4.1	4.5	V	

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.
Note 2: Applies to /CSA, /CSB, E, R/W, DB0~DB7.

4.3 Timing Specifications

At Ta = -20 °C to +70 °C, VDD = 5V±5%, VSS = 0V.

Refer to Fig. 2 MPU read timing diagram and Fig. 3 MPU write timing diagram.

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
E cycle time	t_{CYC}	1000	-	-	ns
E High Level Width	P_{WEH}	450	-	-	ns
E Low Level Width	P_{WEL}	450	-	-	ns
E Rise Time	tr	-	-	25	ns
E Fall Time	tf	-	-	25	ns
Address Setup Time	t_{AS}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Setup Time	t_{DSW}	200	-	-	ns
Data Delay Time	t_{DDR}	-	-	320	ns
Data Hold Time (Write)	t_{DHW}	10	-	-	ns
Data Hold Time (Read)	t_{DHR}	20	-	-	ns

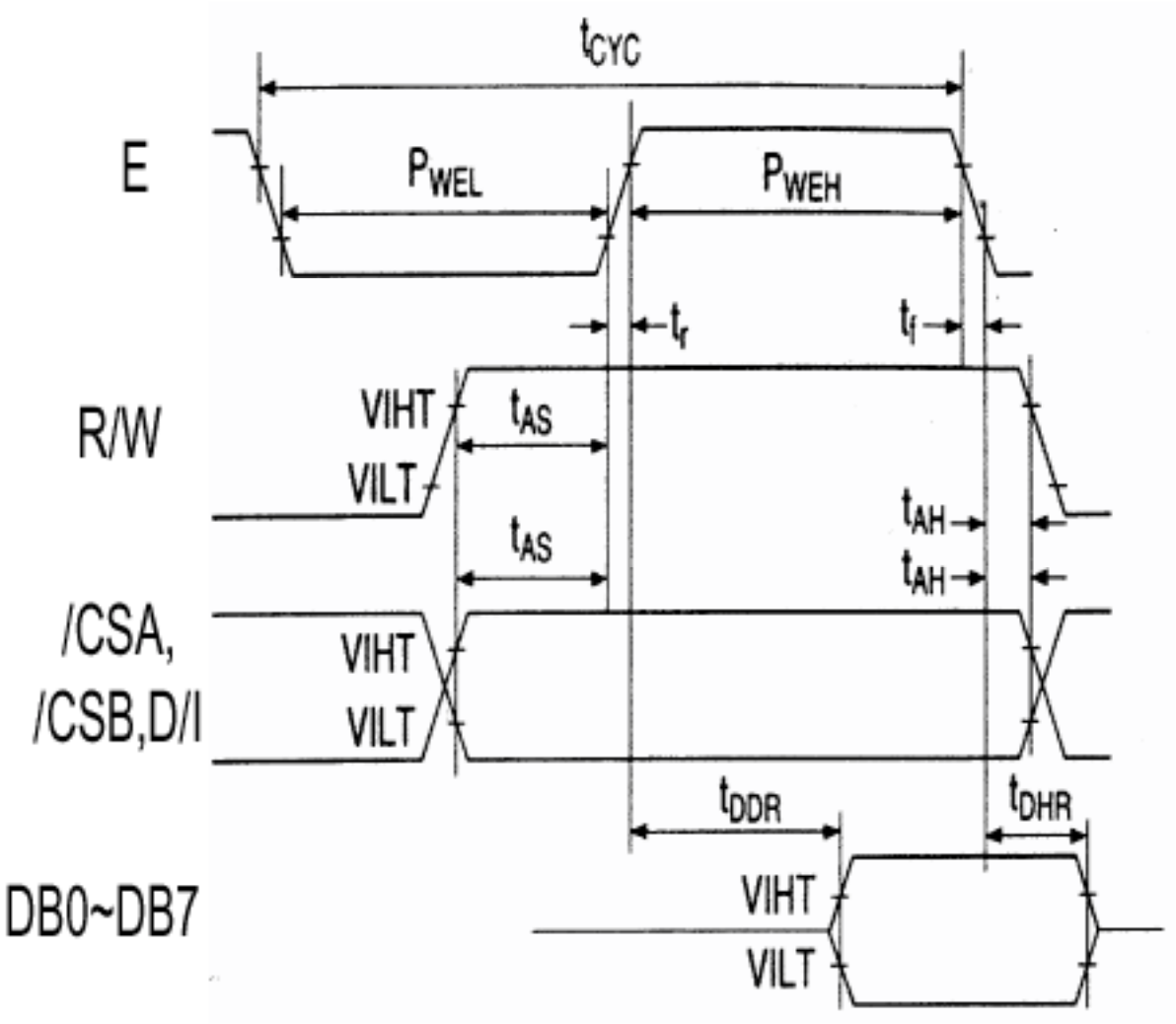

Fig. 2 MPU read timing diagram.

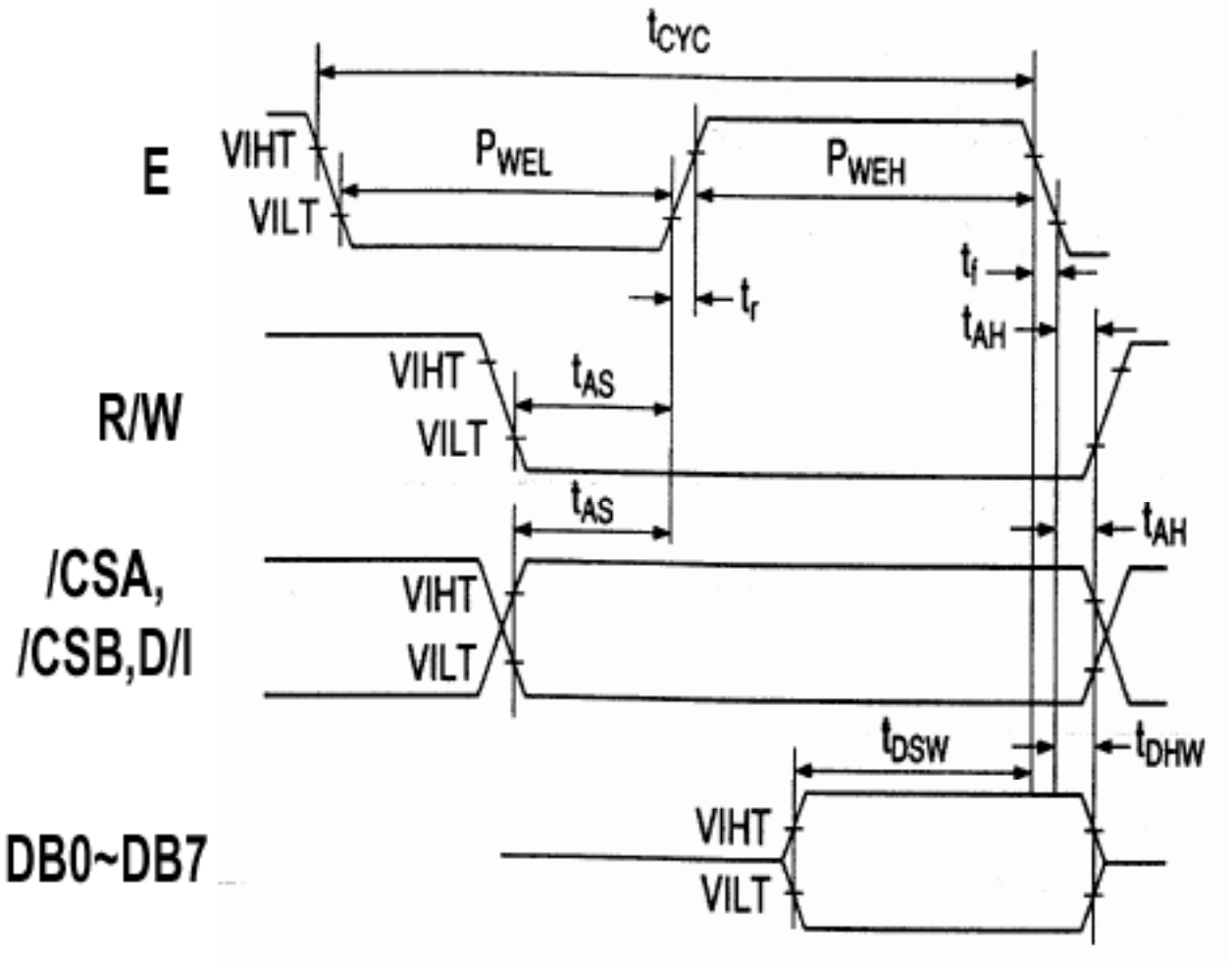

Fig. 3 MPU write timing diagram.

4.4 Timing Diagram of VDD Against Vo.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against Vo.

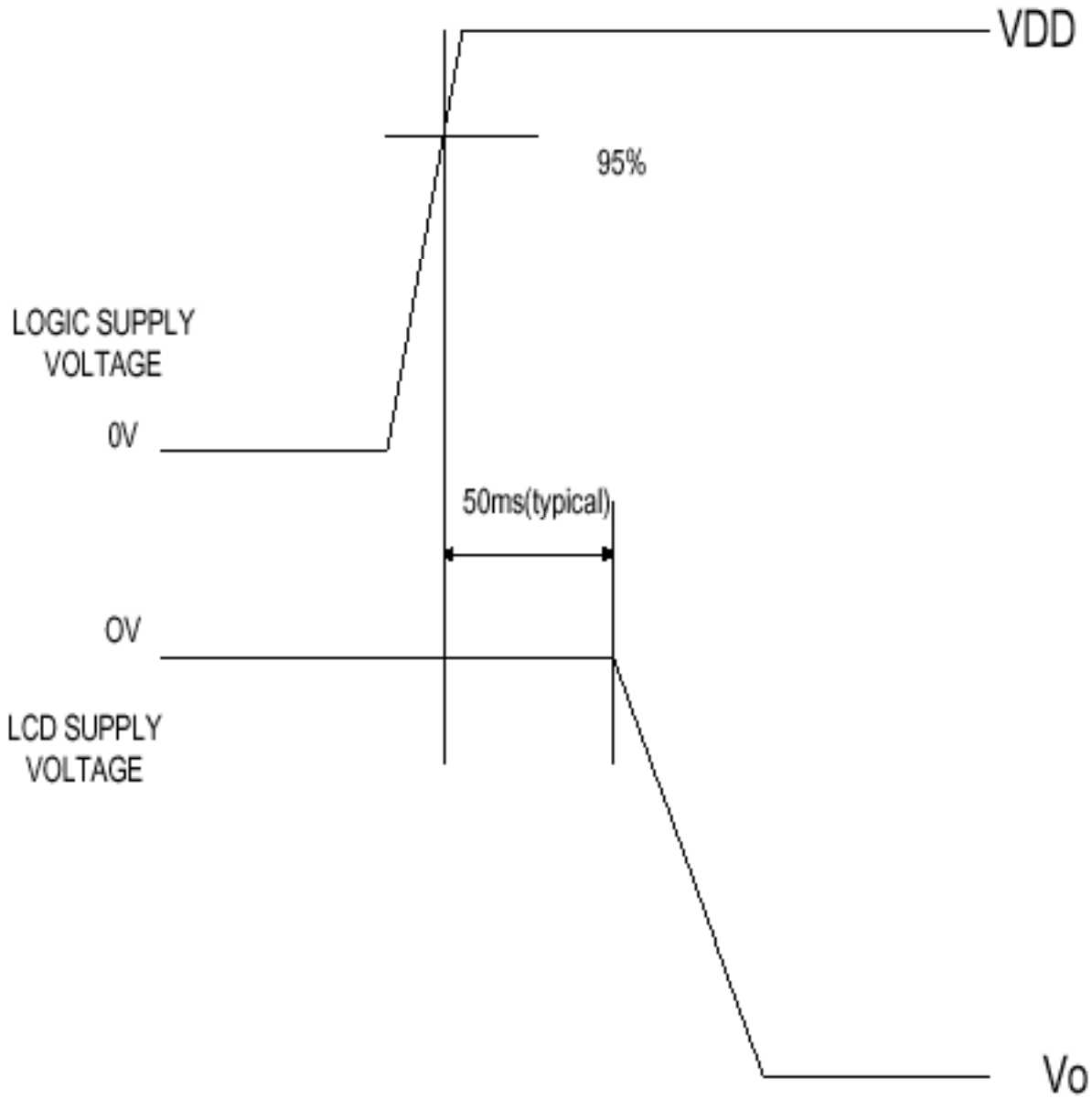

Figure 4: Timing diagram of VDD against Vo.

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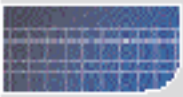

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