PRODUCT DESCRIPTION

Technical Paper
STP 99-12

A NEW SERIAL-CONTROLLED MOTOR-DRIVER IC

by Thomas Truax and Robert Stoddard

ABSTRACT

A new serial-controlled IC has been specifically developed to drive dc motors. This paper will present this new serial-controlled motor driver, which includes several unique circuit design features. These features, which include various current-decay and synchronous rectification modes, and programmable digital timing, will be described in detail. The paper will also discuss the *actual* power dissipation savings that are realized with synchronous rectification of the power DMOS outputs.

INTRODUCTION

For a motor driver IC to drive a wide range of sub-fractional horsepower brush dc motors in a variety of applications, several key device characteristics are required. The motor driver IC requires an H-bridge capable of driving high peak currents and relatively high dc currents. It must accomplish this while limiting the power dissipation to a level low enough to use conventional DIP/SOIC packaging without the need for a heat sink. The IC also needs to have an accurate internal pulse-width modulation (PWM) current-control circuit that can operate in mixed/fast current-decay PWM, to ensure good current regulation, and in slow current-decay PWM to minimize switching losses.

To allow the user to configure many of the timing and control functions with a minimum number of control lines, the IC would have to be serially programmable. A brake function is also needed to passively brake the dc motor by effectively shorting the motor winding.

The motor-driver IC requires an enable input terminal that can be configured through the serial port, to either PWM the device in slow- or fast-decay modes, or brake the motor. This single enable input can also be used as a high-speed PWM control line in voltage-mode, speed-control loops.

Finally, the motor-driver IC requires integrated protection circuitry to prevent device failure due to excessive junction temperatures or low supply voltages.

To meet the above requirements, the A3958 serial-controlled motor-driver IC was developed, providing a flexible and cost-effective solution for driving dc motors. The A3958 is a serial-controlled full-bridge IC, with DMOS outputs capable of continuous output currents of ±2 A and operating voltages to 50 V (see figure 1).

FUNCTIONAL DESCRIPTION

DMOS H-bridge

The outputs of the A3958 are power n-channel DMOS transistors with a typical $r_{DS(on)}$ of 270 mΩ. There are several advantages for driving dc motors with power DMOS transistors. An obvious advantage is the low driver forward-voltage drop and resulting low power dissipation that can be realized with the low $r_{DS(on)}$ rating of the DMOS outputs. Another advantage is the very high peak-current handling characteristic of DMOS transistors, which is particularly advantageous for driving dc motors. Many brush dc motors include a varistor for clamping the voltage spikes that occur when the brushes commutate the motor windings. The capacitive characteristic of this varistor can produce vary large current demands whenever the H-bridge outputs are switched. Another advantage of DMOS is the improved PWM load-current regulation of the internal current-control loop due to the fast switching speed of the DMOS drivers.

Perhaps the biggest advantage of using DMOS power output transistors for motor-driver ICs is the ability to reduce power dissipation by synchronously rectifying the flyback of the inductive load in PWM applications. In PWM applications, the DMOS output drivers are chopped (i.e. turned ON and OFF) at frequencies typically in excess of 20 kHz to regulate the motor's applied voltage

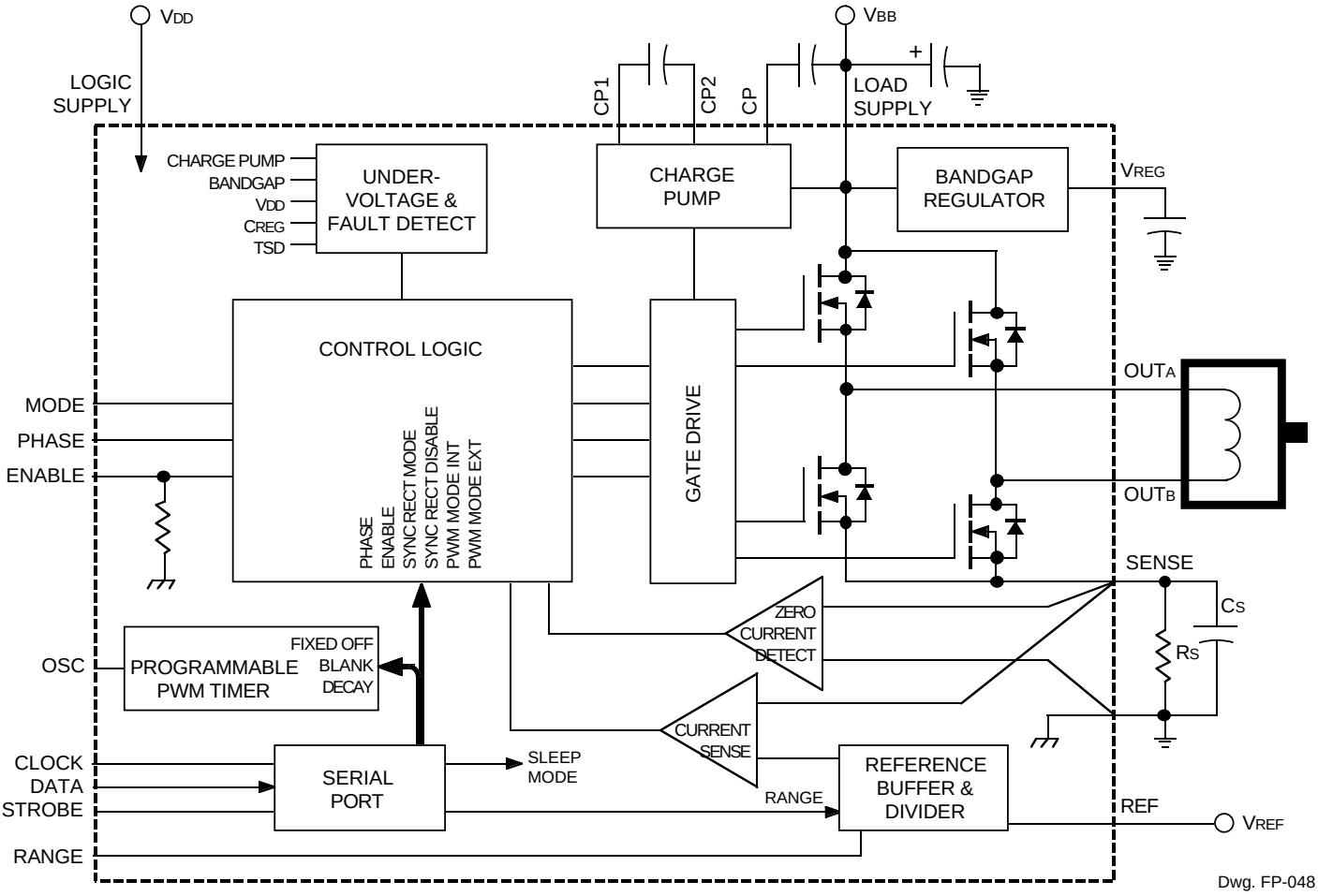

Figure 1: A3958 functional block diagram

and/or current. Due to the inductive nature of the motor winding, when the drivers are chopped off, the inductive flyback of the motor winding is typically clamped by the intrinsic body diode of the DMOS output transistors.

In many PWM systems, the duty cycle of the chopped state can by quite high. Compared to the smaller voltage drop of the DMOS driver, the large body diode forward voltage drop (about 1 V to 1.5 V) can result in a large component of conduction loss. To lower the chopped-state conduction loss, the synchronous rectification control circuitry turns ON the DMOS device in parallel with the conducting body diode.

The operation of the synchronous rectification function is shown in figure 2. The top trace shows the voltage on OUT_A of the A3958. When the source driver is chopped off, the inductive motor winding drives the output voltage below ground, thereby forward basing the body diode of the opposing half-bridge DMOS sink driver (A).

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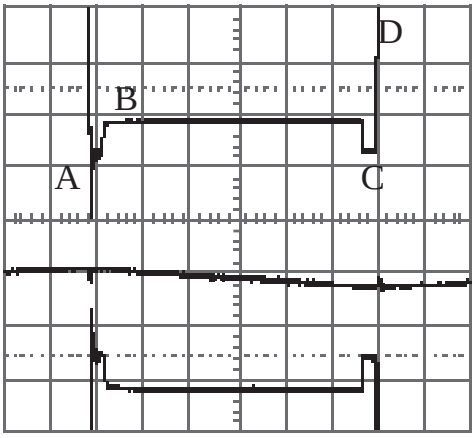

Figure 2: Output waveforms
Top Trace - Sink-side synch. rect., 1 V/div.
Middle Trace - I_{LOAD} ≈1 A, 500 mA/div.
Bottom Trace - Source-side synch. rect., 1 V/div.
Time Scale: 2 µs/div

After a ~700 ns "crossover delay", the synchronous-rectification control circuit turns ON the sink driver resulting in a ~0.6 V decrease in the voltage drop across the device (B). The crossover delay time ensures that shoot-through currents (the simultaneous conduction of a half-bridge sink and source driver) can not occur. At the end of the "off" portion of the PWM cycle, the synchronously rectifying DMOS sink driver is disabled and the body diode again conducts during the crossover delay (C), ensuring that shoot-through current can not occur when the source driver is turned back on (D).

The bottom trace of figure 2 shows the voltage on OUT_B, which shows the synchronous rectification function when the sink driver is chopped off. The inductive load causes the output voltage to rise above the motor supply voltage, thereby forward biasing the opposing source side DMOS driver's body diode. Again the synchronous rectification control circuit can be seen to lower the voltage drop across the device during the chopped portion of the PWM cycle by turning on the high side DMOS driver. For reference, the center trace is the load current, which shows the A3958 operating at 1 A.

Table 1 shows the measured junction temperature rise from the ambient temperature (ΔT_J) for the A3958 operating with synchronous rectification and operating without synchronous rectification. The junction temperature was measured for various load-current levels in both slow current-decay mode and fast current-decay mode. The motor supply voltage (V_{BB}) was 44 V and the chop frequency was 33 kHz.

Table 1

Average Load Current	Decay Mode	ΔT_J with S.R. ON	ΔT_J with S.R. OFF
500 mA	Slow	11.2°C	20.5°C
	Fast	19.1°C	36.6°C
1.0 A	Slow	26.2°C	43.8°C
	Fast	49.9°C	101.5°C
1.5 A	Slow	67.9°C	94.8°C
	Fast	90.0°C	>140°C

As shown above, there is significant power dissipation savings and resulting junction temperature reduction with synchronous rectification of the DMOS outputs. The higher junction temperature in fast current-decay mode compared to slow current-decay mode is due to the higher switching loses in fast current-decay mode.

Because the 5 V nominal logic supply voltage is not sufficient to fully enhance the low-side DMOS drivers, the A3958 includes an internal 8 V linear regulator that runs off the motor supply voltage (V_{BB}). The output of the 8 V regulator is internally monitored to ensure that the DMOS outputs are disabled if the motor supply voltage drops to an unacceptably low level.

An internal charge pump regulator circuit is used to drive the high-side n-channel DMOS transistors. The charge pump generates a gate-source voltage that is sufficiently higher than the motor supply voltage to turn ON the high-side power outputs. Two external capacitors are required: one to act as the "pump", and the other to act as a charge reservoir. This "charge pump" voltage is internally monitored, and the high-side DMOS outputs are disabled if there is not sufficient gate-source voltage available.

Unlike conventional voltage doubling/tripling charge-pump configurations, the charge-pump circuit used in the A3958 is a true regulator incorporating a feedback loop. This circuit configuration has the advantage that the output-current capability of the charge pump is largely invariant with operating frequency. As a result, the charge pump can operate at a low frequency, reducing unwanted EMI.

Current control

The A3958 incorporates a fixed-off time PWM circuit to regulate the current in the winding of a dc motor. Many aspects of the PWM current waveform, such as the off time, blank time, current-decay modes, and synchronous-rectification modes are programmed via the serial port (discussed later).

The A3958 current-control circuitry works as follows: when the outputs of the H-bridge are turned on, current increases in the dc motor winding and is sensed by the current-sense comparator via an external sense resistor (R_S). Current continues to increase until it reaches a trip point that is set by R_S, the applied reference voltage (V_{REF}), and the Range Select level (which is programmed by either the serial port or the RANGE terminal). The current-trip point is either:

$$I_{TRIP} = V_{REF}/10R_S$$

or

$$I_{TRIP} = V_{REF}/5R_S$$

depending on the Range Select level.

At the trip point, the current-sense comparator turns OFF the appropriate output drivers, as determined by the current-decay mode that was set in the serial port. The source driver only is turned OFF for slow current-decay mode, and both the source and sink drivers are turned OFF for mixed and fast current-decay modes. The load inductance of the dc motor causes the current to recirculate for a "fixed-off time" (t_{off}) that also is programmed in the serial port. The path of the current during recirculation is determined by the current-decay mode that was selected. In slow current-decay mode, the source driver is disabled and load current recirculates through both sink drivers (one sink driver is synchronously rectifying). In fast current-decay mode, both the source and sink drivers are disabled and current recirculates via synchronous rectification through the opposite source and sink drivers (see figure 3).

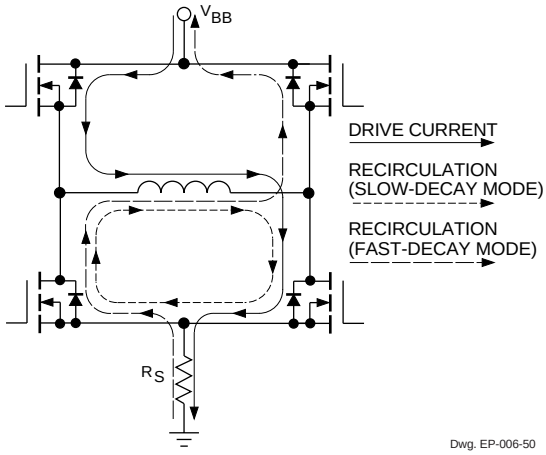

Figure 3: Current paths

During this recirculation, the current decreases until the fixed-off time expires. The appropriate output drivers are enabled again, the motor winding current again increases, and the PWM cycle is repeated.

When a source or sink driver is turned ON, a current spike through the sense resistor can occur due to the reverse recovery currents of the DMOS body diodes and/or the switching transients related to the distributed capacitance of the dc motor (principally due to a varistor). To prevent this current spike from erroneously tripping the current-sense comparator, the current-sense comparator is digitally "blanked" for a period of time. This blank time is also set via the serial port.

Serial Control

The A3958 is controlled via a 3-wire serial port. A serial interface allows a significant amount of programmability, while minimizing terminal count and thus reducing cost. The programmable features allow maximum flexibility in configuring the internal PWM current control circuitry to match the requirements of a specific dc motor.

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A 20-bit word is used to control the various functions of the A3958, including the blank time, the fixed-off time, the portion of fast decay, the synchronous-rectification mode, the current-decay mode, and the V_{REF} range. The serial port can also enable the H-bridge outputs, or put the IC into sleep mode (see table 2).

Table 2: Serial port bits

Bit	Function
D0	Blank Time LSB
D1	Blank Time MSB
D2	Off Time LSB
D3	Off Time Bit 1
D4	Off Time Bit 2
D5	Off Time Bit 3
D6	Off Time MSB
D7	Fast Decay Time Bit LSB
D8	Fast Decay Time Bit 1
D9	Fast Decay Time Bit 2
D10	Fast Decay Time MSB
D11	Sync. Rect. Mode
D12	Sync. Rect. Enable
D13	External PWM Mode
D14	Enable
D15	Phase
D16	Reference Range Select
D17	Internal PWM Mode
D18	Test Use Only
D19	Sleep Mode

Two bits are used to set up the current-sense comparator blank time. Four different blank times can be programmed: $4/f_{OSC}$, $6/f_{OSC}$, $12/f_{OSC}$, or $24/f_{OSC}$, where f_{OSC} is the frequency of an external oscillator. With an oscillator frequency of 4 MHz, the blank time could be set for 1µs, 1.5 µs, 3 µs, or 6 µs.

Five bits are used to set the fixed-off time for the internal PWM current control (figure 4). The off time is defined by the following equation:

$$t_{off} = [8(1+N)/f_{OSC}] - 1/f_{OSC}$$

where N = 0…31.

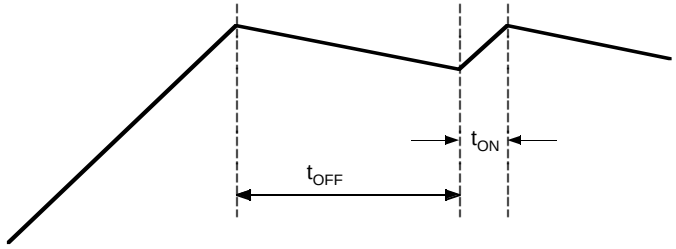

Figure 4: Slow-decay current waveform

Again with a 4 MHz oscillator, the fixed-off time can be programmed from 1.75 µs to 63.75 µs in increments of 2 µs.

Four bits are used to set the fast current-decay portion of the fixed-off time for the internal PWM control circuitry. Fast current-decay will only be in effect if the mixed-decay mode is selected (via either the serial word or the MODE input terminal). If the mixed-decay mode is selected, the portion of the fixed-off time that will be in fast decay is defined by:

$$t_{fd} = [8(1 + N)/f_{OSC}] - 1/f_{OSC}$$

where N = 1…15.

With an oscillator frequency of 4 MHz, the fast decay time can selected from 1.75 µs to 31.75 µs in increments of 2 µs.

If mixed-decay mode is selected and $t_{fd} < t_{off}$, then the A3958 PWM current-control circuitry is operating in mixed-decay mode (figure 5) – i.e. a portion of the off-time will be in fast-decay mode (t_{fd}) and the balance will be in slow decay mode ($t_{slow} = t_{off} - t_{fd}$).

If mixed-decay mode is selected and $t_{fd} > t_{off}$, then the A3958 PWM current control circuitry is operating in fast-decay mode – i.e., it is in fast-decay mode 100% of the off-time (figure 6).

Because the oscillator rising edges are asynchronous to the point at which the load current reaches the I_{TRIP} level, a small amount of jitter, equal to the period of one clock cycle, is introduced in the actual off time. Because the oscillator frequency is high, this jitter term has no observable affect on the load-current waveform.

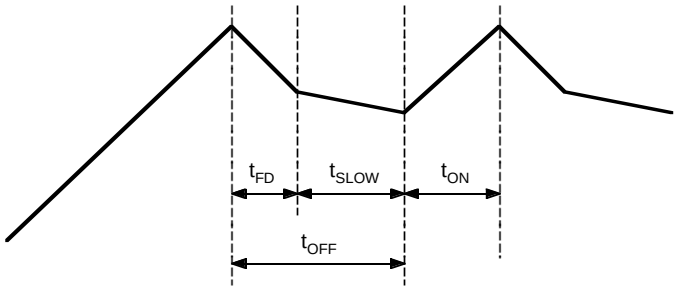

Figure 5: Mixed-decay current waveform

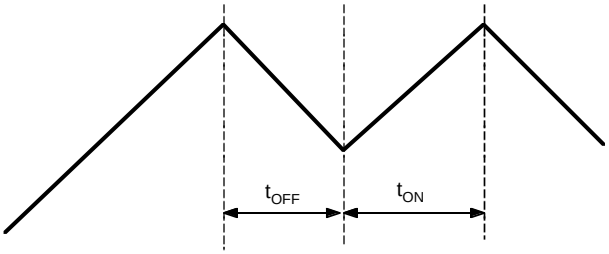

Figure 6: Fast-decay current waveform

One bit in the serial port determines the synchronous rectification mode: active mode or passive mode. If the DMOS outputs are chopped in fast-decay mode, passive synchronous-rectification mode will keep the opposing synchronously rectifying DMOS drivers turned ON until the end of the OFF portion of the PWM cycle. If the OFF time is long enough or the device is operating at low load-current levels, the load current will invert due to synchronously rectifying drivers. To ensure that the inverted load current does not run away, the synchronously rectifying drivers are switched OFF if the inverted load current reaches the I_{TRIP} current limit set for the internal PWM control loop.

An example of the load-current waveform produced during passive-mode synchronous rectification is shown in figure 7. The A3958 is regulating load current with the internal current-control circuit operating in fast current-decay mode. The zero current level for the load current is indicated by the underscore on the trace 4 marker. In this case, the load current can be seen to invert near the end of the OFF portion of the PWM cycle.

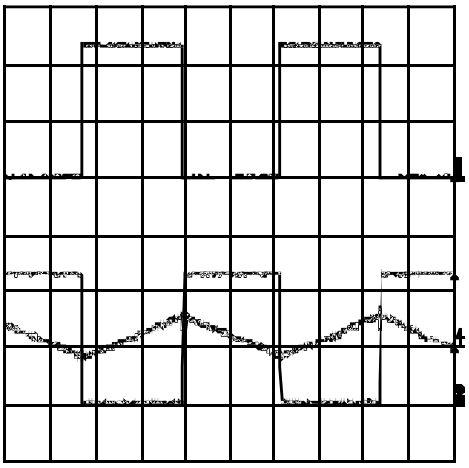

Figure 7: Passive-mode sync. rect.
Trace 1 - OUT_A, 20 V/div.
Trace 2 - OUT_B, 20 V/div.
Trace 4 - Load current, 500 mA/div.
Time Scale: 10 µs/div.

In active synchronous-rectification mode, the opposing synchronously rectifying DMOS drivers are also turned ON during fast decay chopping. However, in active synchronous-rectification mode, the current through the current-sense resistor is monitored to detect if the load current has decayed to zero. If the load current reaches zero, the synchronously rectifying drivers are switched OFF, thus preventing the inversion of the load current.

An example of the load-current waveform produced during active-mode synchronous rectification is shown in figure 8. Inversion of the load current is prevented, resulting in discontinuous load-current conduction. The output voltages oscillate sinusoidally for the remainder of the off time due to the tank circuit formed by the inductive load and capacitance of the output drivers.

Passive synchronous-rectification mode has the advantage that it produces a more linear transconductance function at low current levels. This can be desirable in some servo motor applications because it can simplify the compensation of speed and/or position control loops. Active synchronous-rectification mode has the advantage that the load current polarity is always known, preventing

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potential erroneous load-current inversion when the motor driver is intended to be "OFF".

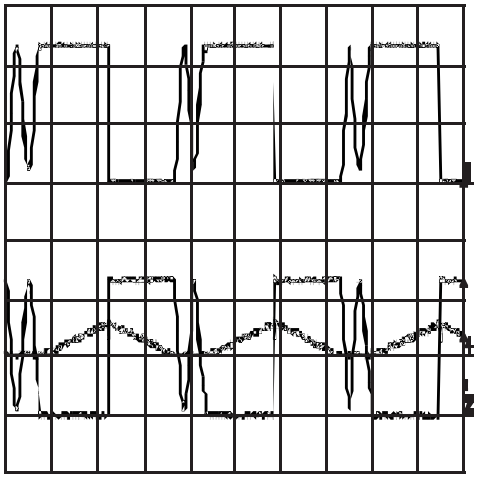

Figure 8: Active-mode sync. rect.
Trace 1 - OUT_A, 20 V/div.
Trace 2 - OUT_B, 20 V/div.
Trace 4 - Load current, 500 mA/div.
Time Scale: 10 μs/div.

One bit of the serial port enables the synchronous-rectification circuitry (both active and passive modes). For most applications, the synchronous-rectification function is typically used to lower the device operating temperature (as previously shown in table 1). In very high current and high duty-cycle applications, external Schottky diodes can be used to lower the heat rise of the A3958. In these extreme power applications, the synchronous-rectification function can be disabled, thereby allowing the external Schottky diodes to conduct the full load current during recirculation and achieve the maximum junction temperature reduction in the IC.

One bit each is used for enable logic, phase logic, range select, and current-decay mode. Consequently, the enable logic, phase logic, range select, and current-decay mode can be controlled by the serial port or the ENABLE, PHASE, RANGE, and MODE terminals. ENABLE chops the output drivers, and PHASE determines the direction of load current in the H-bridge.

One bit is used to put the A3958 into a sleep mode. Sleep mode disables most of the internal circuitry, including the internal regulator and charge-pump circuit. In sleep mode, the logic supply current is typically less than 1 mA, and the motor supply current is less than 20 μA.

A final bit is used to put the A3958 into a test mode. The internal charge pump and V_{REG} monitoring circuits are disabled, allowing for easier testing of the other circuit functions.

Protection Circuitry

An under-voltage lockout circuit protects the A3958 from potential shoot-through currents when the load-supply voltage is applied before the logic-supply voltage. All outputs are disabled until the logic-supply voltage is above 4.2 V, at which time the system control logic is assumed to be able to correctly control the state of the device. At power-up, the serial port data bits are set to zero.

Thermal protection circuitry turns OFF all the power outputs if the junction temperature exceeds 165°C. As with most integrated thermal shutdown circuits, this is intended only to protect the A3958 from failure due to excessive junction temperature and will not necessarily protect the IC from output short circuits. Normal operation is resumed when the junction temperature has decreased about 15°C.

Packaging

To minimize cost, the A3958 is packaged in standard DIP and SOIC packages. The serial interface has reduced the necessary input terminals to allow the A3958 to be packaged in JEDEC standard 24-pin DIP and 24-lead SOIC packages. Both packages have a copper "batwing" tab for improved power dissipation. The 24-pin batwing DIP package has a $R_{\theta JA}$ rating of 40°C/W, while the 24-lead SOIC batwing package has a $R_{\theta JA}$ rating of 56°C/W. These packages provide sufficient power-dissipation capability for many dc motor applications, especially because the A3958 features low $r_{DS(on)}$ DMOS outputs and synchronous rectification.

APPLICATIONS

Figure 9 shows a typical application circuit for the A3958 driving a dc motor. Figure 10 shows an actual current waveform of the A3958 in slow current-decay mode, figure 11 shows an actual current waveform in fast current-decay mode, and figure 12 shows actual current waveforms in mixed-decay mode. In all cases, the load current is approximately 1 A.

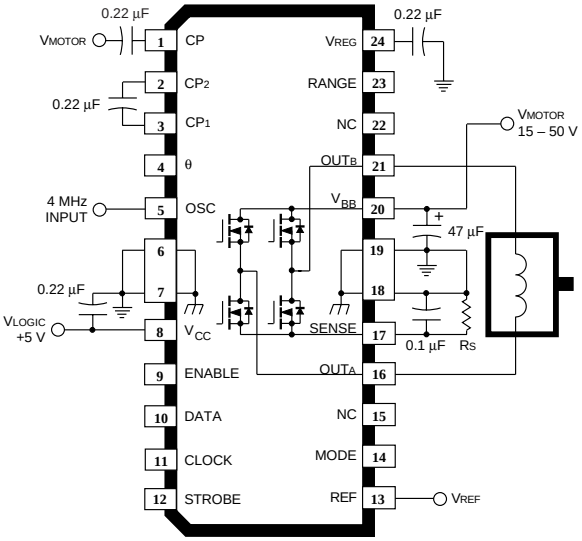

Figure 9: Typical application driving a dc motor

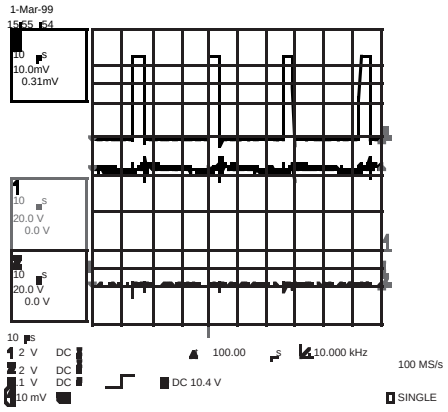

Figure 10: Slow current-decay waveform

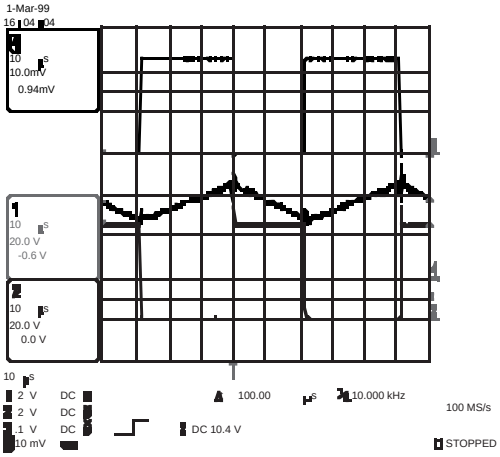

Figure 11: Fast current-decay waveform

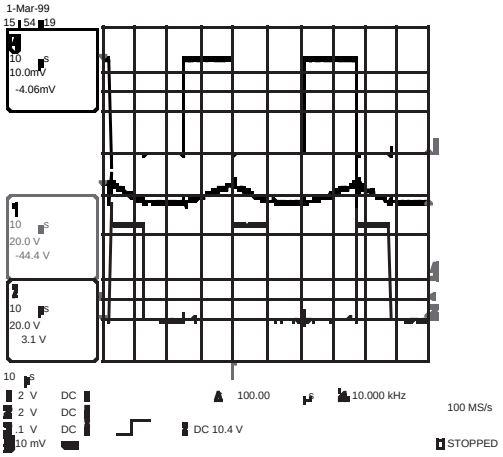

Figure 12: Mixed current-decay waveform

Brake

When the A3958 is chopped in slow current-decay mode, both sink drivers will be ON due to synchronous rectification. If the load is a rotating brush dc motor, and the outputs are held in the chopped state for a time period much longer than the L/R time constant of the load, the back electromotive force (BEMF) will cause the load current to invert. The inverse current will rise to a value determined by the BEMF voltage divided by the resistance of the motor winding.

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This inverse current produces torque opposing the rotation of the motor, thereby effectively braking the motor.

ABCD3

The A3958 is fabricated on Allegro MicroSystems' new ABCD3 (*A*llegro *B*ipolar *C*MOS *D*MOS 3rd generation) process. ABCD3 combines on one IC: bipolar logic circuits, low voltage CMOS logic, and power DMOS transistors. ABCD3 features 70 V vertical DMOS transistors, as well as 35 V and 12 V lateral DMOS transistors. This two-level metal, mixed-signal power technology is based upon a 1.2 µm line-width.

CONCLUSION

A new serial-controlled motor driver has been developed that is able to drive a wide range of brush dc motors in a variety of applications. The A3958, shown in figure 13, combines a power DMOS H-bridge with the flexibility of serially programmable control circuitry to provide a new solution for driving dc motors.

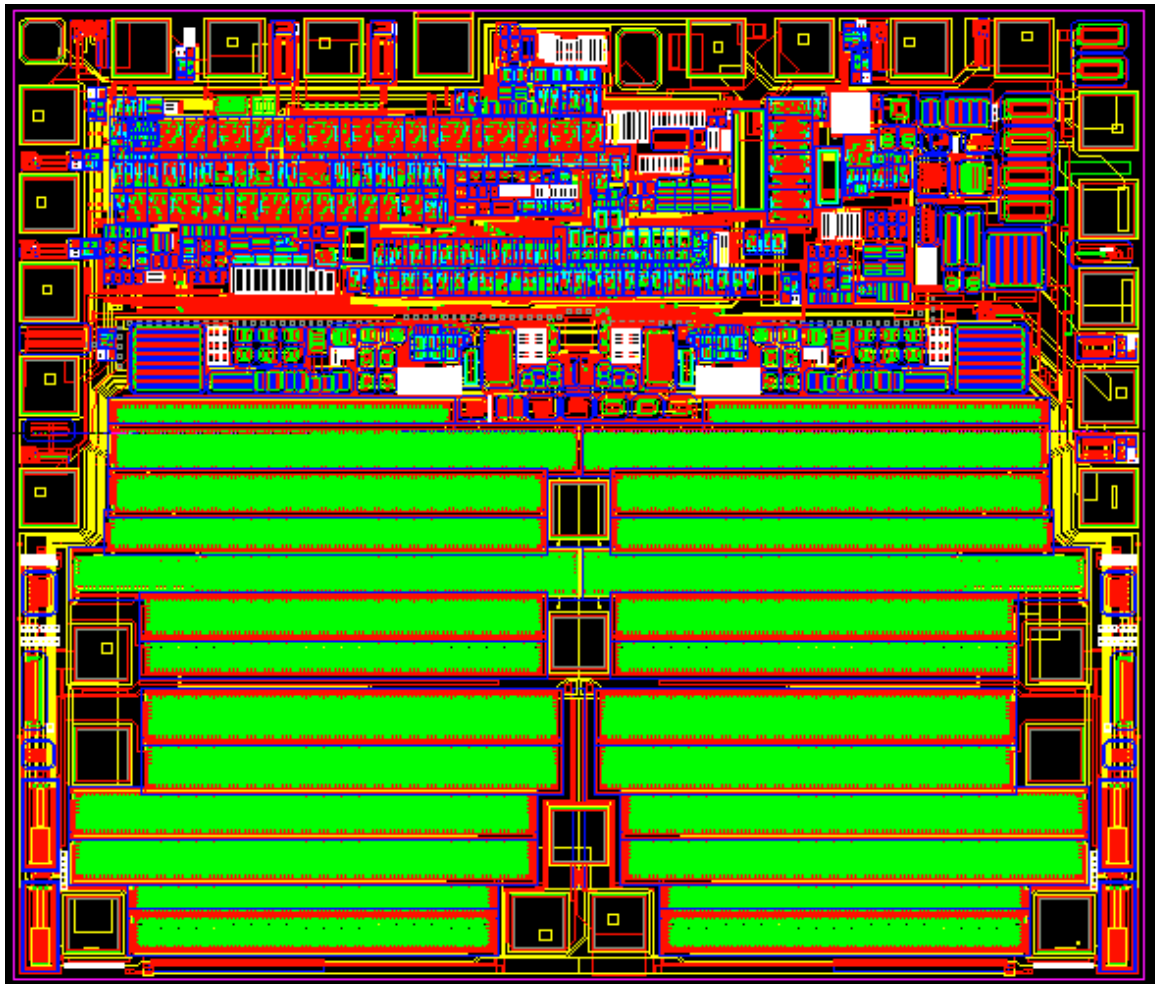

Figure 13: A3958 die layout

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